TPS5420 2A 宽输入范围降压转换器

1 特性

- 宽泛的输入电压：5.5V 至 36V
- 高达 2A 的连续（3A 峰值）输出电流
- 通过 110mΩ 集成式 MOSFET 开关实现高达 95% 的高效率
- 宽输出电压范围：可调节为低至 1.22V，初始精度为 1.5%
- 内部补偿可最大限度减少外部器件数量
- 适用于小型滤波器尺寸的固定 500kHz 开关频率
- 通过输入电压前馈改进线路稳压和瞬态响应
- 系统受过流限制、过压保护和热关断的保护
- -40°C 至 125°C 的工作结温范围
- 采用小型 8 引脚 SOIC 封装

2 应用

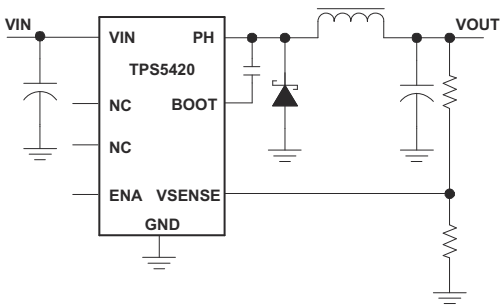
- 消费类电子：机顶盒、DVD、LCD 显示屏
- 工业用和车载音频电源
- 电池充电器、大功率 LED 电源
- 12V/24V 分布式电源系统

3 说明

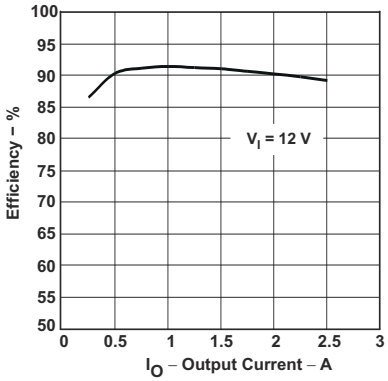
TPS5420 是一款高输出电流的 PWM 转换器，集成了低电阻高侧 N 沟道 MOSFET。具有所列特性的基板上还包括高性能电压误差放大器（可在瞬态条件下提供高稳压精度）、欠压锁定电路（用于防止在输入电压达到 5.5V 前启动）、内部设置的慢启动电路（用于限制浪涌电流）以及电压前馈电路（用于改进瞬态响应）。通过使用 ENA 引脚，关断电源电流通常可减少到 18 μA。其他特性包括高电平有效使能端、过流限制、过压保护和热关断。为降低设计复杂性并减少外部元件数量，TPS5420 反馈环路进行了内部补偿。

TPS5420 器件采用易于使用的 8 引脚 SOIC 封装。TI 提供评估模块和 Designer 软件工具，协助快速实现高性能电源设计，满足迫切的设备开发周期要求。

Simplified Schematic



Efficiency vs Output Current



4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

Table of Contents

5 Ordering Information

T_J	INPUT VOLTAGE	OUTPUT VOLTAGE	PACKAGE(2)	PART NUMBER
– 40°C to 125°C	5.5 V to 36 V	Adjustable to 1.22 V	SOIC (D)(1)	TPS5420D

(1) The D package is available taped and reeled. Add an R suffix to the device type (i.e., TPS5420DR).
(2) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI web site at www.ti.com.

6 Pin Assignments

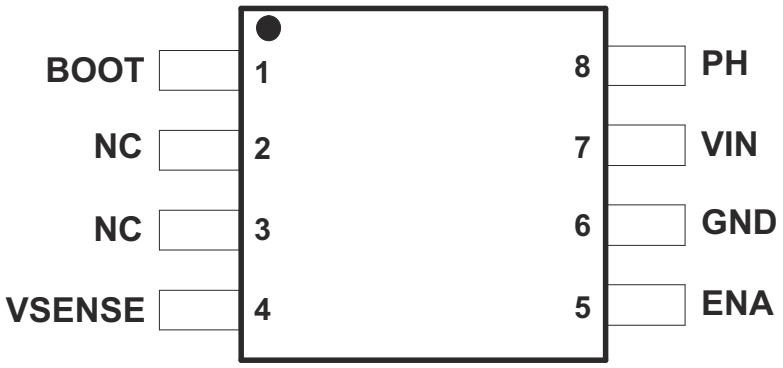


图 6-1. D PACKAGE (TOP VIEW)

6.1 Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
BOOT	1	Boost capacitor for the high-side FET gate driver. Connect 0.01 μF low ESR capacitor from BOOT pin to PH pin.
NC	2, 3	Not connected internally.
VSENSE	4	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	Ground.
VIN	7	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high quality, low ESR ceramic capacitor.
PH	8	Source of the high side power MOSFET. Connected to external inductor and diode.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN(2) to GND	– 0.3	40	V
Input voltage	ENA to GND	– 0.3	7	V
Input voltage	VSENSE to GND	– 0.3	3	V
Output voltage	BOOT to PH	– 0.3	6	V
Output voltage	BOOT to GND	– 0.3		V
Output voltage	PH to GND, (Steady-state)(2)	– 0.6	40	V
Output voltage	PH to GND, (transient < 10ns)	– 1.2		V
Source current	PH		Internally Limited	
Source current	PH Leakage current		10	µA
T_J	Operating virtual junction temperature	– 40	150	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	Input voltage range	5.5		36	V
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS5420 D (SOIC) 8 PINs	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (Custom Board)(2)	75	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7)	106	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56	°C/W

THERMAL METRIC(1)		TPS5420 D (SOIC) 8 PINs	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*
(2) Refer to the TPS5420's EVM User's Guide for board layout and additional information. For thermal design information please see the Maximum Ambient Temperature section.

7.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 5.5 V to 36 V. Typical values are at T_J = 25°C and V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{SENSE} = 2 V, PH pin open		2	4.4	mA
$I_{SD(VIN)}$	VIN shutdown supply current	Shutdown, ENA = 0 V		15	50	µA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{VIN} rising		5.3	5.5	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.35		V
VOLTAGE REFERENCE						
V_{FB}	FB voltage	T_J = 25°C	1.202	1.221	1.239	V
V_{FB}	FB voltage	T_J = –40°C to 125°C	1.196	1.221	1.245	V
OSCILLATOR						
f_{SW}	Switching frequency		400	500	600	kHz
$t_{ON(min)}$	Minimum ON pulse width			150	200	ns
D_{MAX}	Maximum Duty Cycle	f_{SW} = 500kHz	85%	89%		
ENABLE (ENA PIN)						
$V_{EN(R)}$	ENA voltage rising threshold				1.3	V
$V_{EN(F)}$	ENA voltage falling threshold		0.5			V
$V_{EN(H)}$	ENA voltage hysteresis			325		mV
t_{SS}	Internal slow-start time (0~100%)		6.6	8	10	ms
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit		3	4	5	A
	Hiccup time before re-start		13	16	20	ms
OUTPUT MOSFET						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 12 V, $V_{BOOT-SW}$ = 4.5 V		100	230	mΩ
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 5.5 V, $V_{BOOT-SW}$ = 4.0 V		125		mΩ
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (1)	Temperature rising	135	162		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			14		°C

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters. Not production tested.

7.6 Typical Characteristics

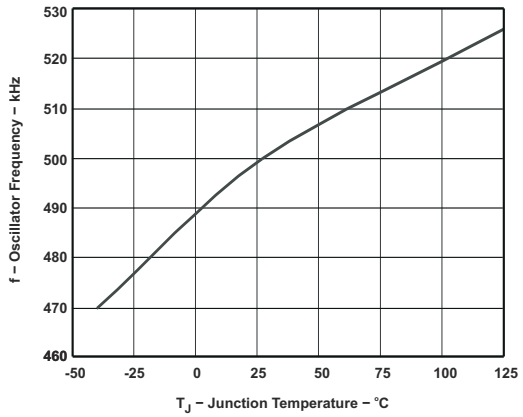


图 7-1. OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

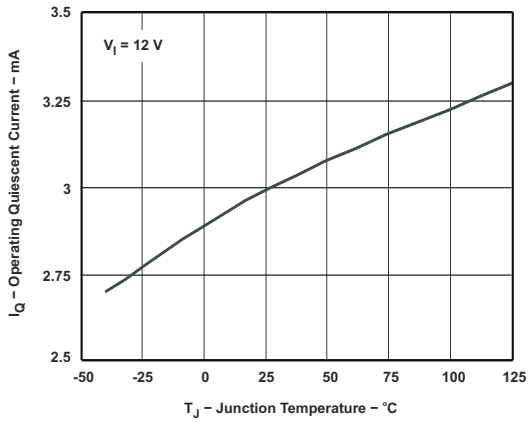


图 7-2. OPERATING QUIESCENT CURRENT vsJUNCTION TEMPERATURE

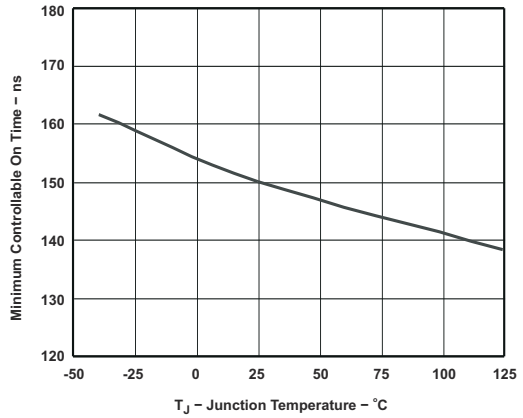


图 7-3. MINIMUM CONTROLLABLE ON TIME vsJUNCTION TEMPERATURE

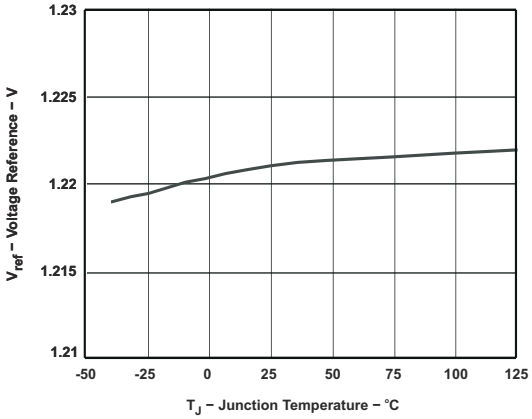


图 7-4. VOLTAGE REFERENCE vsJUNCTION TEMPERATURE

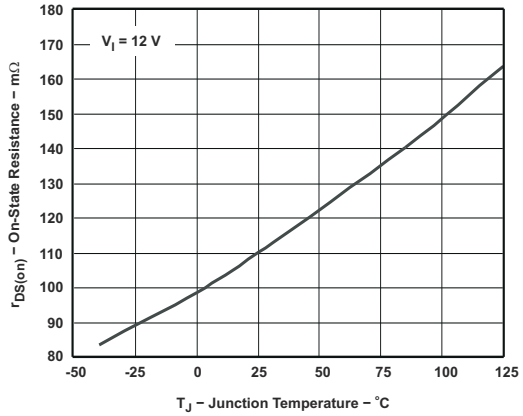


图 7-5. ON STATE RESISTANCE vsJUNCTION TEMPERATURE

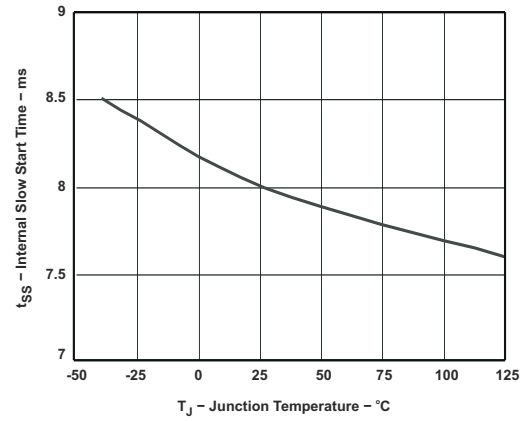


图 7-6. INTERNAL SLOW START TIME vsJUNCTION TEMPERATURE

7.6 Typical Characteristics (continued)

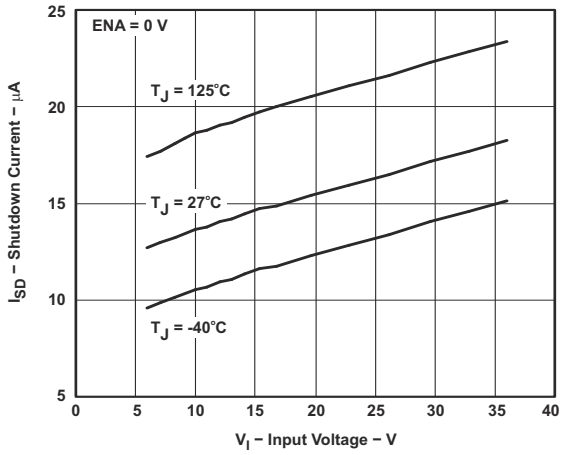


图 7-7. SHUTDOWN QUIESCENT CURRENT vs INPUT VOLTAGE

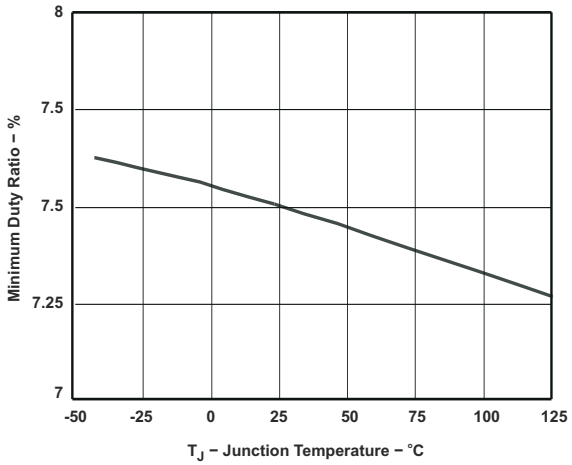
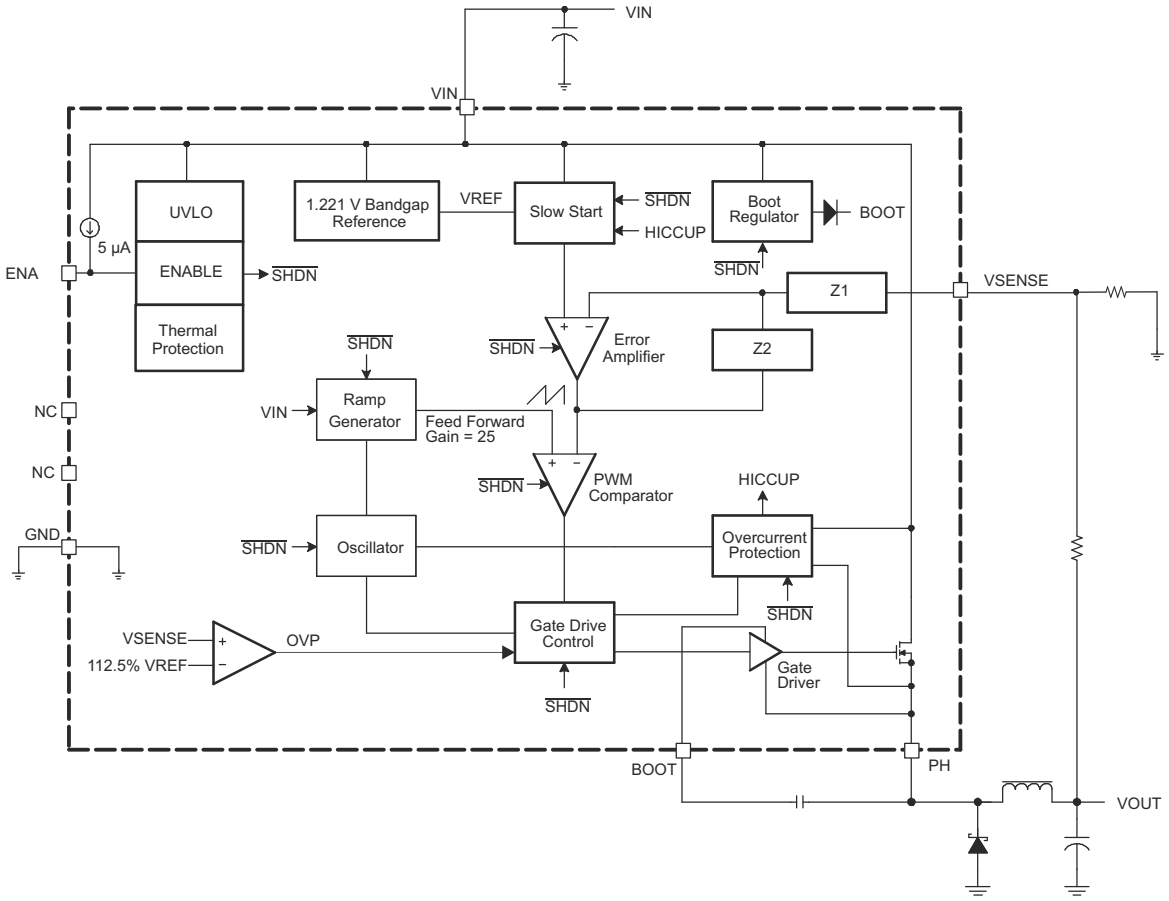


图 7-8. MINIMUM CONTROLLABLE DUTY RATIO vs JUNCTION TEMPERATURE

8 Application Information

8.1 Functional Block Diagram



8.2 Detailed Description

8.2.1 Oscillator Frequency

The internal free running oscillator sets the PWM switching frequency at 500 kHz. The 500 kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

8.2.2 Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

8.2.3 Enable (ENA) and Internal Slow Start

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.5 V disables the regulator and activate the shutdown mode. The quiescent current of the TPS5420 in shutdown mode is typically 18 µA.

The ENA pin has an internal pullup current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit

the start-up inrush current, an internal slow start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. The internal slow start time is 8 ms typically.

8.2.4 Undervoltage Lockout (UVLO)

The TPS5420 incorporates an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

8.2.5 Boost Capacitor (BOOT)

Connect a 0.01 μF low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

8.2.6 Output Feedback (VSENSE)

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage should be equal to the voltage reference 1.221 V.

8.2.7 Internal Compensation

The TPS5420 implements internal compensation to simplify the regulator design. Since the TPS5420 uses voltage mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Internal Compensation Network* in the applications section for more details.

8.2.8 Voltage Feed Forward

The internal voltage feed forward provides a constant DC power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feed forward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed forward gain, i.e.

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk-pk}}} \quad (1)$$

The typical feed forward gain of TPS5420 is 25.

8.2.9 Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error voltage magnitude is converted to a pulse width which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

8.2.10 Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system will ignore the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting scheme is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used, i.e. hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow start circuit.

8.2.11 Overvoltage Protection

The TPS5420 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% x VREF. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET will be forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

8.2.12 Thermal Shutdown

The TPS5420 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

8.2.13 PCB Layout

Connect a low ESR ceramic bypass capacitor to the VIN pin. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS5420 ground pin. The best way to do this is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7 µF ceramic with a X5R or X7R dielectric.

There should be a ground area on the top layer directly underneath the IC to connect the GND pin of the device and the anode of the catch diode. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown in 图 8-1.

The PH pin should be routed to the output inductor, catch diode and boot capacitor. Since the PH connection is the switching node, the inductor should be located close to the PH pin, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings may also be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, Lout, Cout and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pinout, the trace may need to be routed under the output capacitor. The routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If the grounding scheme shown is used via a connection to a different layer to route to the ENA pin.

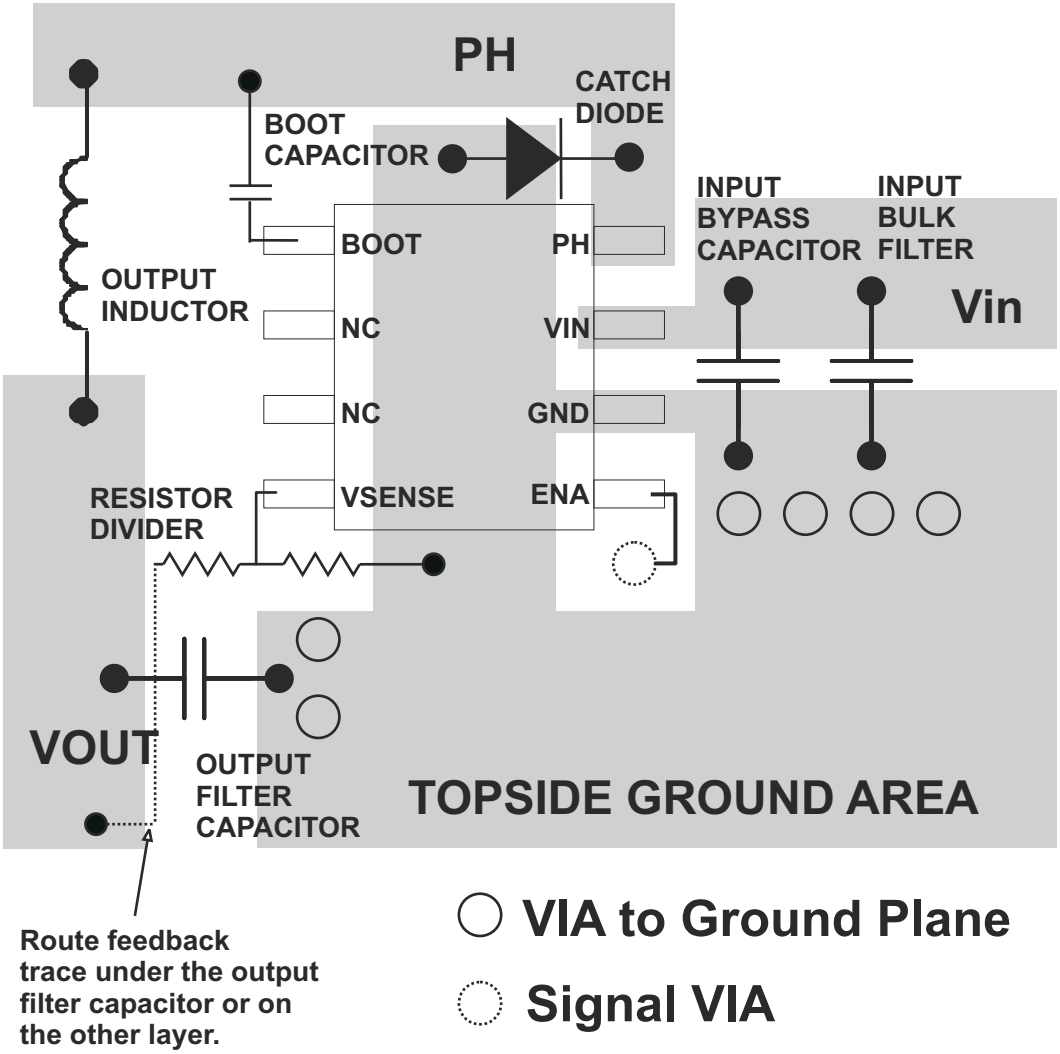


图 8-1. Design Layout

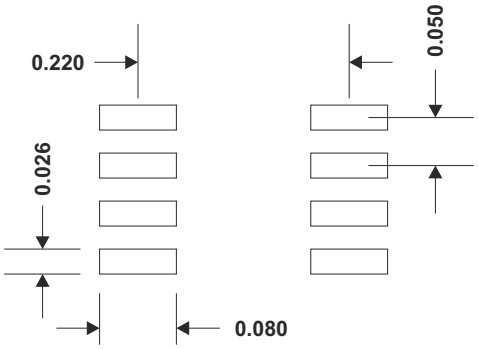
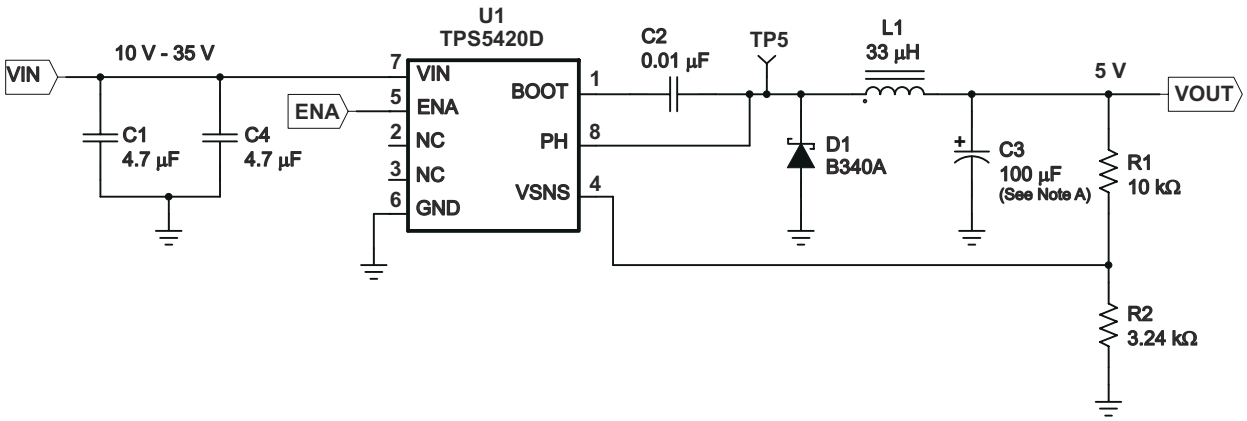


图 8-2. TPS5420 Land Pattern

8.2.14 Application Circuits

图 8-3 shows the schematic for a typical TPS5420 application. The TPS5420 can provide up to 2-A output current at a nominal output voltage of 5 V.



A. C3 = Tantalum AVX TPSD107M010R0080

图 8-3. Application Circuit, 10-V — 35 V to 5-V

8.2.15 Design Procedure

The following design procedure can be used to select component values for the TPS5420. Alternately, the Designer Software may be used to generate a complete design. The Designer Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

To begin the design process, a few parameters must be determined. The designer must know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

8.2.15.1 Design Parameters

For this design example, use the following as the input parameters:

DESIGN PARAMETER(1)	EXAMPLE VALUE
Input voltage range	10 V to 36 V
Output voltage	5 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	2 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

8.2.15.2 Switching Frequency

The switching frequency for the TPS5420 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

8.2.15.3 Input Capacitors

The TPS5420 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The recommended value for the decoupling capacitor is 10 μF. A high quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, if the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple. For this design, two 4.7 μF capacitors, C1 and C4 are used to allow for smaller 1812 case size to be used while maintaining a 50 V rating.

This input ripple voltage can be approximated by 方程式 2 :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_I is the input capacitor value and ESR_{MAX} is the maximum series resistance of the input capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this is approximated by 方程式 3:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (3)$$

In this example, the calculated input ripple voltage is 118 mV, and the RMS ripple current is 1.0 A. The maximum voltage across the input capacitors would be VIN max plus delta VIN/2. The chosen input decoupling capacitors are rated for 50 V, and the ripple current capacity for each is 3 A at 500 kHz, providing ample margin. The actual measured input ripple voltage may be larger than the calculated value due to the output impedance of the input voltage source and parasitics associated with the layout.

> **小心**
>
> The maximum ratings for voltage and current are not to be exceeded under any circumstance.

Additionally, some bulk capacitance may be needed, especially if the TPS5420 circuit is not located within approximately 2 inches from the input voltage source. The value for this capacitor is not critical but it should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

8.2.15.4 Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Since the TPS5420 is an internally compensated device, a limited range of filter component types and values can be supported.

8.2.15.4.1 Inductor Selection

To calculate the minimum value of the output inductor, use 方程式 4:

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{OUT} \times F_{SW} \times 0.8} \quad (4)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak to peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current, and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5420, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages is obtained when paired with the proper output capacitor, the peak switch current is below the current limit set point, and low load currents can be sourced before discontinuous operation.

For this design example, use K_{IND} = 0.2, and the minimum inductor value is 27 μH. The standard value used in this design is 33 μH.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from 方程式 5:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \quad (5)$$

and the peak inductor current can be determined using 方程式 6:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (6)$$

For this design, the RMS inductor current is 2.002 A, and the peak inductor current is 2.16 A. The chosen inductor is a Coilcraft MSS1260-333 type. The nominal inductance is 33 μH. It has a saturation current rating of

2.2 A and a RMS current rating of 2.7 A, which meets the requirements. Inductor values for use with the TPS5420 are in the range of 10 μH to 100 μH.

8.2.15.4.2 Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor ripple current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is recommended to keep the closed loop crossover frequency in the range 3 kHz to 30 kHz as this frequency range has adequate phase boost to allow for stable operation. For this design example, the intended closed loop crossover frequency is between 2590 Hz and 24 kHz, and below the ESR zero of the output capacitor. Under these conditions, the closed loop crossover frequency is related to the LC corner frequency as:

$$f_{CO} = \frac{f_{LC}^{2}}{85\ V_{OUT}} \tag{7}$$

and the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \tag{8}$$

For a desired crossover of 18 kHz and a 33-μH inductor, the calculated value for the output capacitor is 100 μF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR is:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \tag{9}$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}(MAX) = \frac{ESR_{MAX} \times V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8} \tag{10}$$

Where:

ΔV_{PP} is the desired peak-to-peak output ripple.

N_C is the number of parallel output capacitors.

F_{SW} is the switching frequency.

The minimum ESR of the output capacitor should also be considered. For a good phase margin, if the ESR is zero when the ESR is at its minimum, it should not be above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by 方程式 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8 \times N_C} \right] \quad (11)$$

Where:

N_C is the number of output capacitors in parallel.

F_{SW} is the switching frequency.

For this design example, a single 100- μF output capacitor is chosen for C3. The calculated RMS ripple current is 143 mA and the maximum ESR required is 88 mΩ. A capacitor that meets these requirements is a AVX TPSD107M010R0080, rated at 10 V with a maximum ESR of 80 mΩ and a ripple current rating of 1.369 A. This capacitor results in a peak-to-peak output ripple of 26 mV using equation 10. An additional small 0.1- μF ceramic bypass capacitor may also used, but is not included in this design.

Other capacitor types can be used with the TPS5420, depending on the needs of the application.

8.2.15.5 Output Voltage Setpoint

The output voltage of the TPS5420 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 5 V using 方程式 12:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \quad (12)$$

For any TPS5420 design, start with an R1 value of 10 kΩ. R2 is then 3.24 kΩ.

8.2.15.6 Boot Capacitor

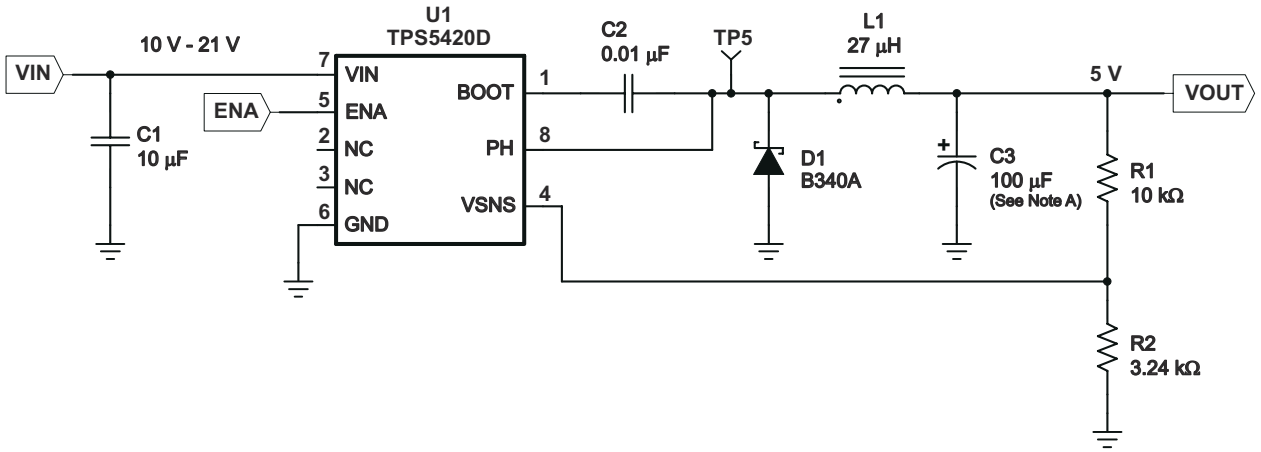
The boot capacitor should be 0.01 μF.

8.2.15.7 Catch Diode

The TPS5420 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is VINMAX + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak-to-peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time; therefore, the diode parameters improve the overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B340A is chosen, with a reverse voltage of 40 V, forward current of 3 A, and a forward voltage drop of 0.5 V.

8.2.15.8 Additional Circuits

图 8-4 shows an application circuit using a wide input voltage range. The design parameters are similar to those given for the design example, with a larger value output inductor and a lower closed loop crossover frequency.



A. C3 = Tantalum AVX TPSD107M010R0080

图 8-4. 10-V — 21-V Input to 5-V Output Application Circuit

8.2.15.9 Circuit Using Ceramic Output Filter Capacitors

图 8-5 shows an application circuit using all ceramic capacitors for the input and output filters which generates a 3.3-V output from a 10-V to 24-V input. The design procedure is similar to those given for the design example, except for the selection of the output filter capacitor values and the design of the additional compensation components required to stabilize the circuit.

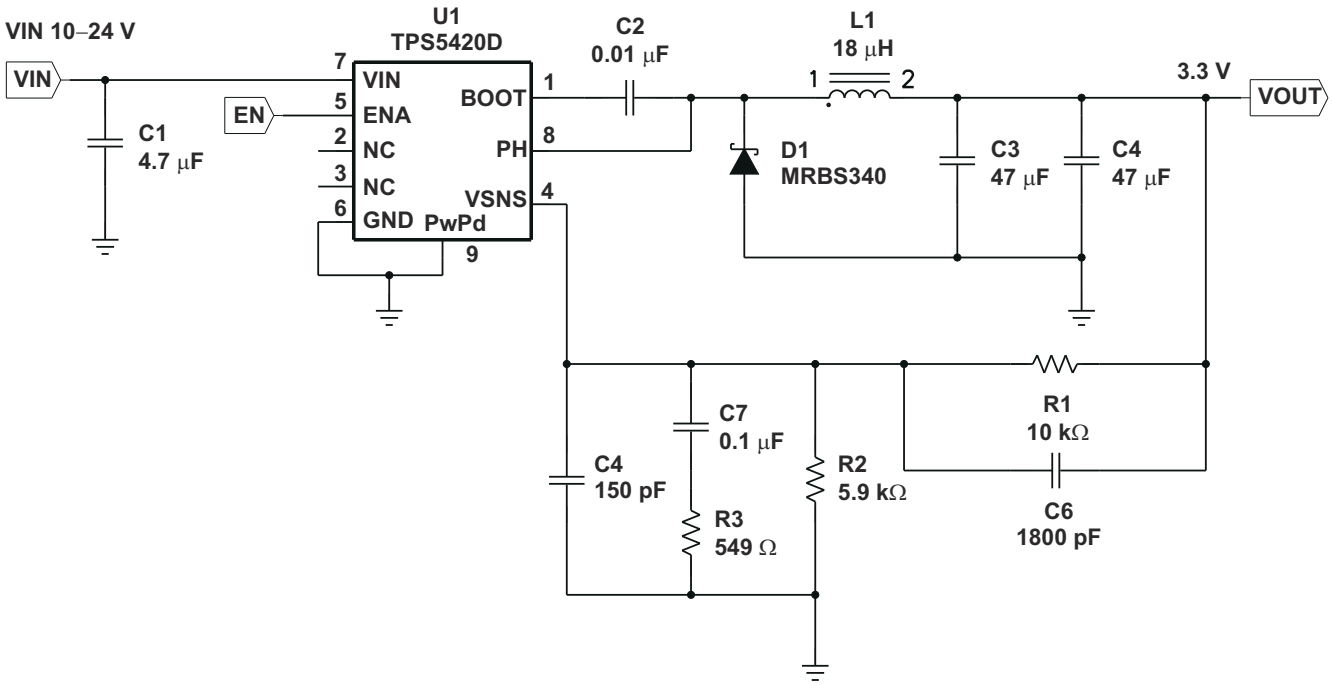


图 8-5. Ceramic Output Filter Capacitors Circuit

8.2.15.10 Output Filter Component Selection

Using 方程式 11, the minimum inductor value is 17.9 µH. A value of 18 µH is chosen for this design.

When using ceramic output filer capacitors, the recommended LC resonant frequency should be no more than 7 kHz. Since the output inductor is already selected at 18 µH, this limits the minimum output capacitor value to:

$$C_O\,(MIN) \geq \frac{1}{(2\pi \times 7000)^2 \times L_O} \quad (13)$$

The minimum capacitor value is calculated to be 29 μF. For this circuit a larger value of capacitor yields better transient response. Two 47 μF output capacitors are used for C3 and C4. It is important to note that the actual capacitance of ceramic capacitors decreases with applied voltage. In this example, the output voltage is set to 3.3 V, minimizing this effect.

8.2.15.11 External Compensation Network

When using ceramic output capacitors, additional circuitry is required to stabilize the closed loop system. For this circuit, the external components are R3, C5, C6, and C7. To determine the value of these components, first calculate the LC resonant frequency of the output filter:

$$F_{LC} = \frac{1}{2\pi \sqrt{L_O \times C_O\,(EFF)}} \quad (14)$$

For this example the effective resonant frequency is calculated as 4109 Hz

The network composed of R1, R2, R3, C5, C6, and C7 has two poles and two zeros that are used to tailor the overall response of the feedback network to accommodate the use of the ceramic output capacitors. The pole and zero locations are given by the following equations:

$$Fp1 = 500000 \times \frac{V_O}{F_{LC}} \quad (15)$$

$$Fz1 = 0.7 \times F_{LC} \quad (16)$$

$$Fz2 = 2.5 \times F_{LC} \quad (17)$$

The final pole is located at a frequency too high to be of concern. The second zero, Fz2 as defined by 方程式 17 uses 2.5 for the frequency multiplier. In some cases this may need to be slightly higher or lower. Values in the range of 2.3 to 2.7 work well. The values for R1 and R2 are fixed by the 3.3-V output voltage as calculated using 方程式 12. For this design R1 = 10 kΩ and R2 = 5.90 kΩ. With Fp1 = 426 Hz, Fz1 = 2708 Hz and Fz2 = 8898 Hz, the values of R3, C6 and C7 are determined using 方程式 18, 方程式 19, and 方程式 20:

$$C7 = \frac{1}{2\pi \times Fp1 \times (R1 \parallel R2)} \quad (18)$$

$$R3 = \frac{1}{2\pi \times Fz1 \times C7} \quad (19)$$

$$C6 = \frac{1}{2\pi \times Fz2 \times R1} \quad (20)$$

For this design, using the closest standard values, C7 is 0.1 μF, R3 is 590 Ω, and C6 is 1800 pF. C5 is added to improve load regulation performance. It is effectively in parallel with C6 in the location of the second pole frequency, so it should be small in relationship to C6. C5 should be less the 1/10 the value of C6. For this example, 150 pF works well.

For additional information on external compensation of the TPS5420 or other wide voltage range devices, see SLVA237 *Using TPS5410/20/30/31 With Aluminum/Ceramic Output Capacitors*

8.3 Advanced Information

8.3.1 Output Voltage Limitations

Due to the internal design of the TPS5420, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230\right) + V_D\right) - \left(I_{OMAX} \times R_L\right) - V_D \quad (21)$$

Where:

V_{INMIN} = minimum input voltage

I_{OMAX} = maximum load current

V_D = catch diode forward voltage.

R_L= output inductor series resistance.

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110\right) + V_D\right) - \left(I_{OMIN} \times R_L\right) - V_D \quad (22)$$

Where:

V_{INMAX} = maximum input voltage

I_{OMIN} = minimum load current

V_D = catch diode forward voltage.

R_L= output inductor series resistance.

This equation assumes nominal on resistance for the high side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be checked to assure proper functionality.

8.3.2 Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS5420. These designs are based on certain assumptions, and always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS5420. 方程式 23 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)} \quad (23)$$

Where

Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz

Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz

Fp3 represents the non-ideal parasitics effect.

Using this information along with the desired output voltage, feed forward gain and output filter characteristics, the closed loop transfer function can be derived.

8.3.3 Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: $Pcon = I_{OUT}^{2} \times R_{DS(on)} \times V_{OUT} / V_{IN}$

Switching Loss: $Psw = V_{IN} \times I_{OUT} \times 0.01$

Quiescent Current Loss: $Pq = V_{IN} \times 0.01$

Total Loss: $Ptot = Pcon + Psw + Pq$

Given T_A => Estimated Junction Temperature: $T_J = T_A + Rth \times Ptot$

Given T_{JMAX} = 125°C => Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX} - Rth \times Ptot$

8.4 Performance Graphs

The performance graphs in 图 8-6 - 图 8-12 are applicable to the circuit in 图 8-3. T_A = 25°C. unless otherwise specified.

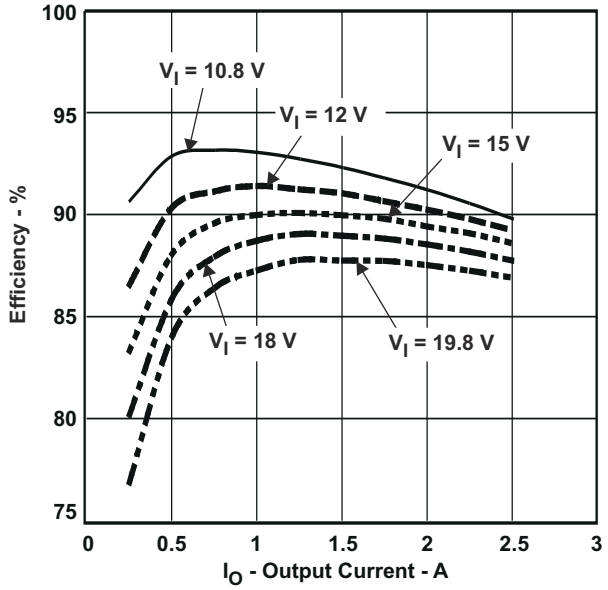


图 8-6. Efficiency vs. Output Current

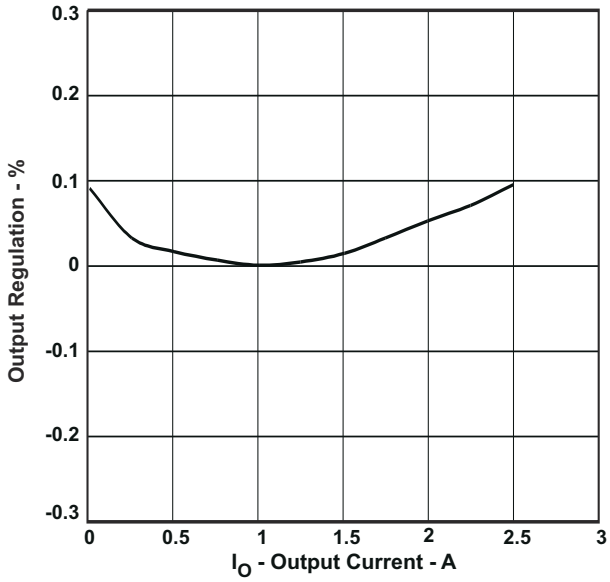


图 8-7. Output Regulation % vs. Output Current

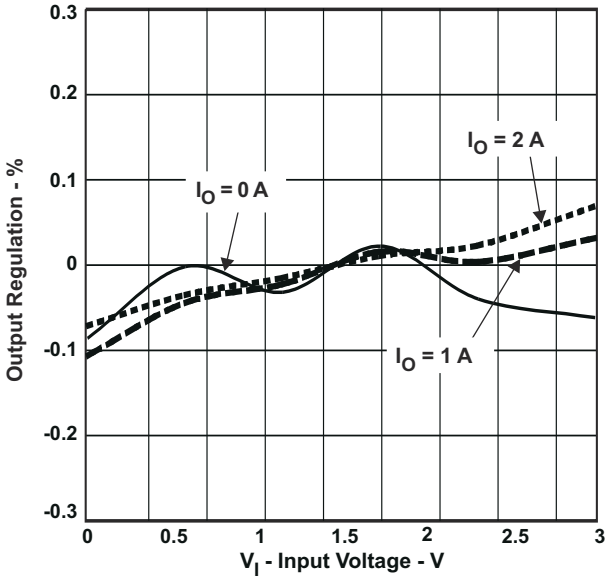


图 8-8. Input Regulation % vs. Input Voltage

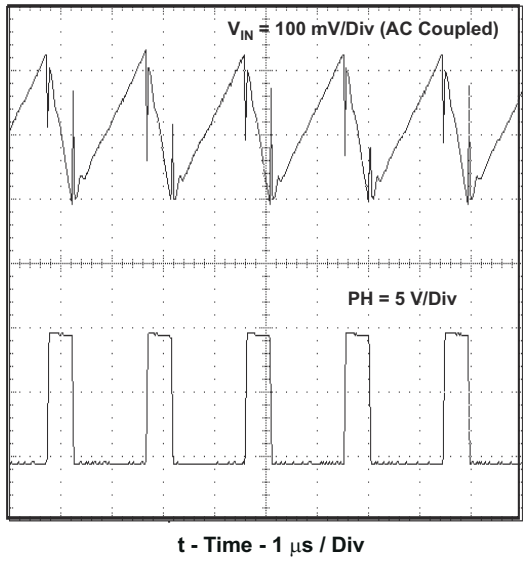


图 8-9. Input Voltage Ripple and PH Node, I_O = 3 A

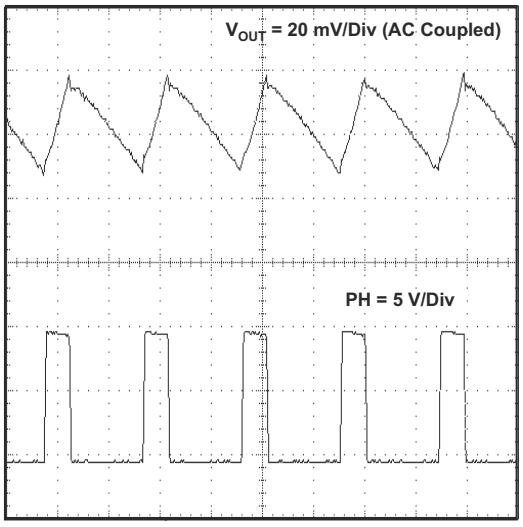


图 8-10. Output Voltage Ripple and PH Node, I_O = 3 A

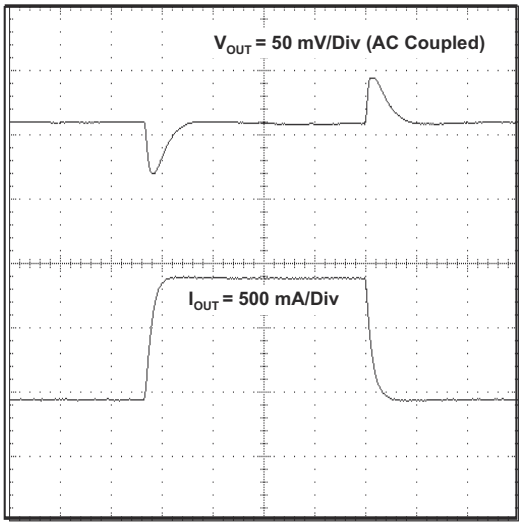


图 8-11. Transient Response, Io Step 0.5 to 1.5 A

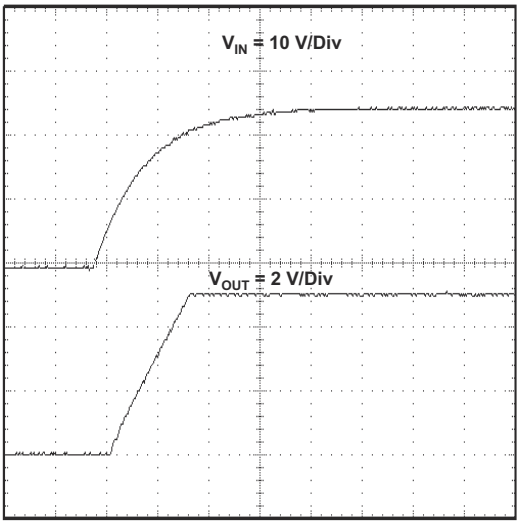


图 8-12. Startup Waveform, V_{IN} and V_{OUT}

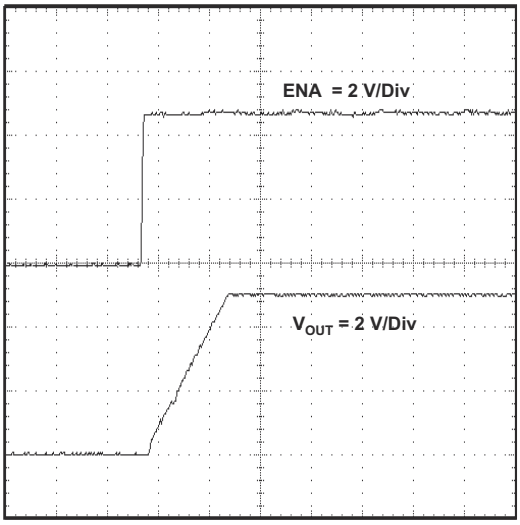


图 8-13. Startup Waveform, ENA and V_{OUT}

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (September 2013) to Revision F (January 2024) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Updated to new format which does not include specific parameter names and does include min and max columns. TJ called out in header. Pin names are used rather than signal names. BOOT and PH voltages now marked as output voltage. Footnotes updated and Note 2 removed 5
- Changed BOOT to PH Absolute Maximum to 6 V maximum 5
- Deleted Absolute Maximum BOOT to GND maximum voltage 5
- Added ESD table 5
- Added Recommended operating V_I input voltage 5
- Updated footnotes to match current TI standards, replaced custom board specifications with EVM information and JEDEC standard information 5
- Changed $R_{\theta JC(top)}$, $R_{\theta JB}$, ψ_{JT}, ψ_{JB} 5
- Added condition for typical specifications EC table’s header, added parameter names, and used pin names in parameter descriptions. Footnote added 6
- Updated the following test conditions: V_{FB}, D_{MAX}, and $R_{DSON(HS)}$ 6
- Updated the following typical specifications in the EC table: $I_{Q(VIN)}$, $I_{SD(VIN)}$, $VIN_{UVLO(H)}$, $V_{EN(H)}$, and $R_{DSON(HS)}$ 6

Changes from Revision D (January 2013) to Revision E (September 2013) **Page**

- 删除了数据表标题、特性和说明中的 SWIFT 1

Changes from Revision C (October 2007) to Revision D (January 2013) **Page**

- Replaced the DISSIPATION RATINGS with the THERMAL INFORMATION table 5

Changes from Revision B (November 2006) to Revision C (October 2007) **Page**

- Changed From: K_{IND} = 0.2, and the minimum inductor value is 31 µH To: K_{IND} = 0.2, and the minimum inductor value is 27 µH 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5420D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5420	Samples
TPS5420DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5420	Samples
TPS5420DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5420	Samples
TPS5420DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS5420	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS5420 :

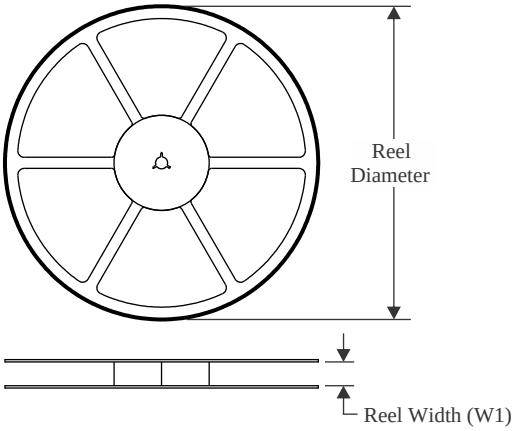
- Automotive : TPS5420-Q1
- Enhanced Product : TPS5420-EP

NOTE: Qualified Version Definitions:

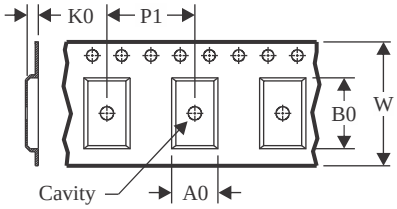
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

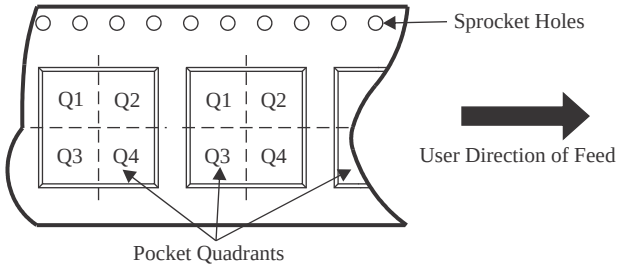


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

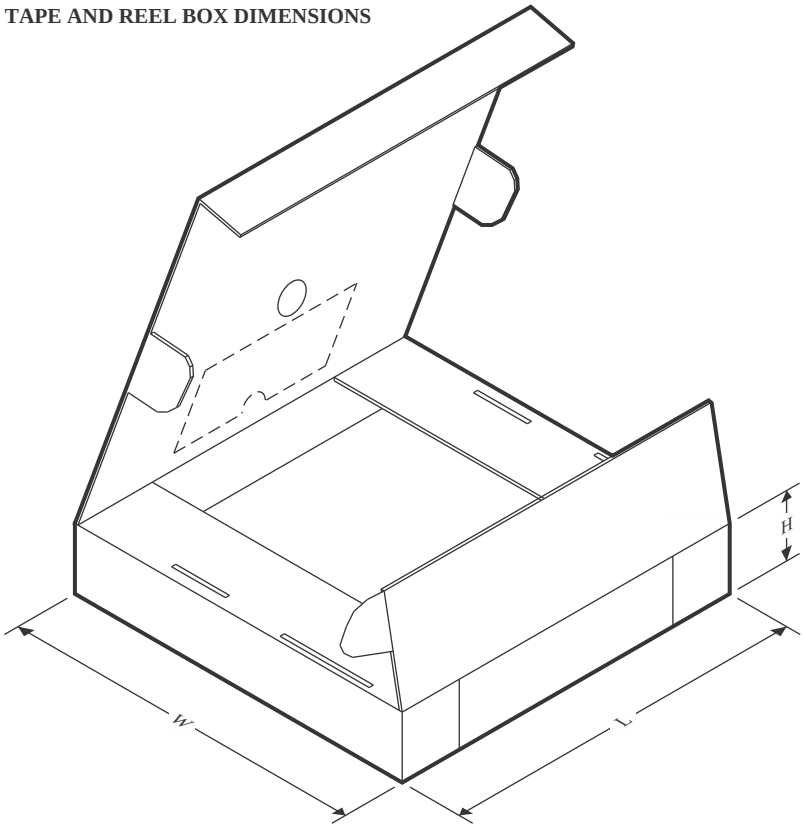
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5420DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

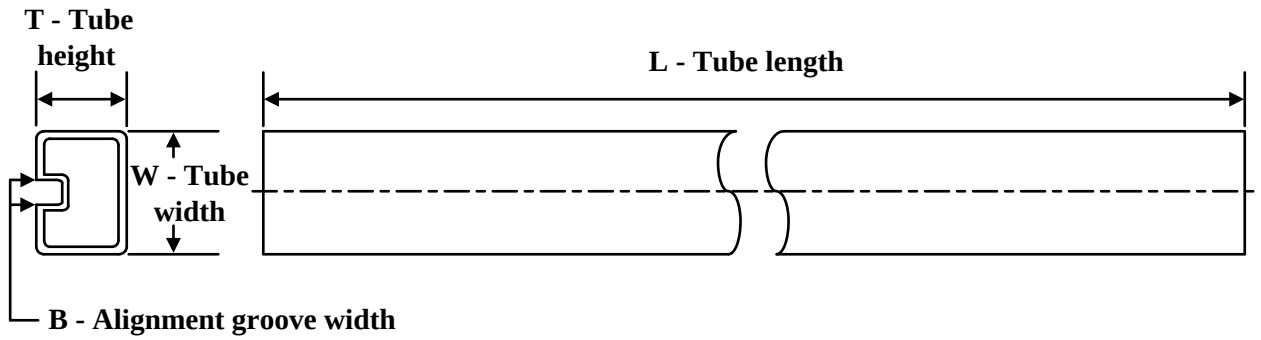
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

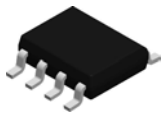
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5420DR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS5420D	D	SOIC	8	75	506.6	8	3940	4.32
TPS5420DG4	D	SOIC	8	75	506.6	8	3940	4.32

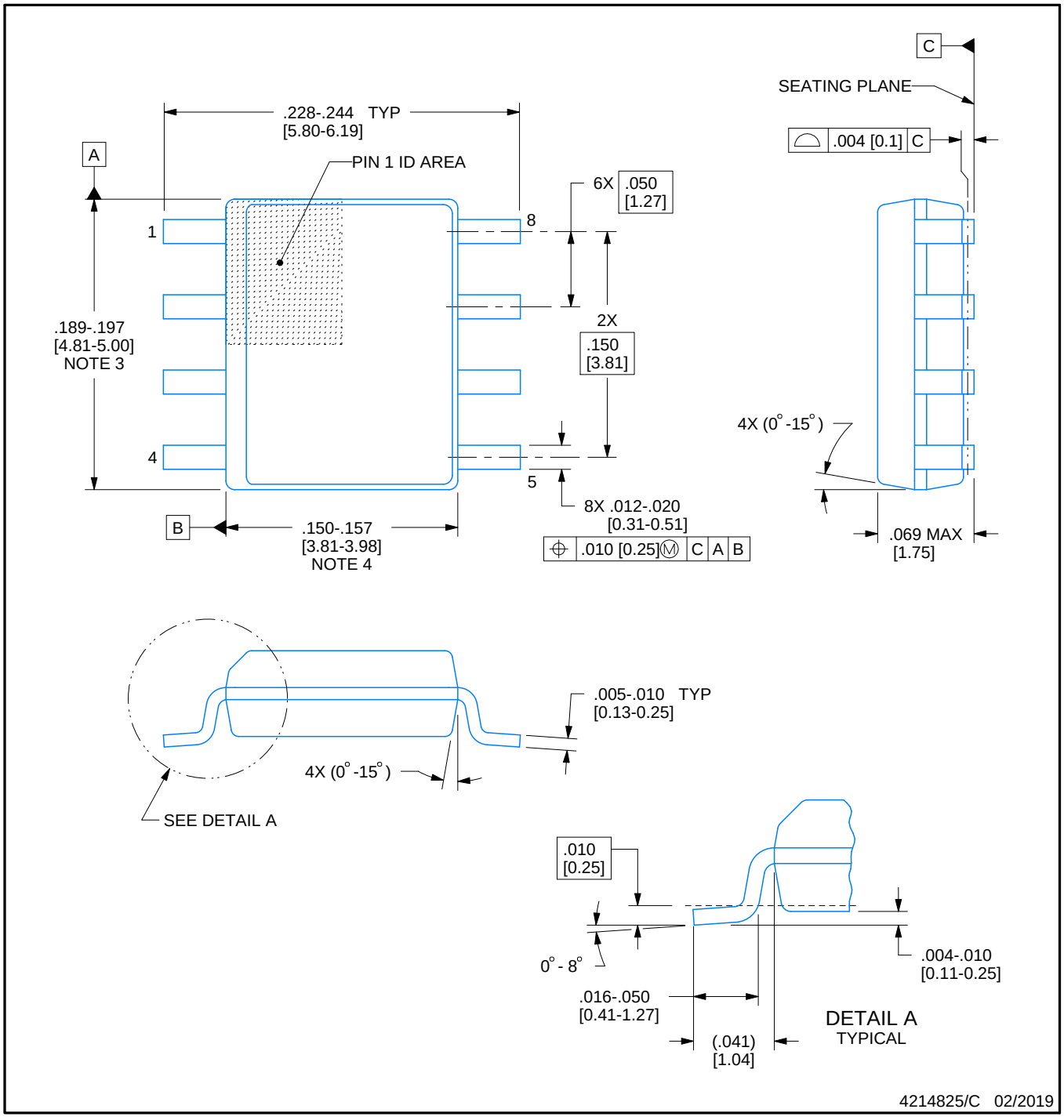


PACKAGE OUTLINE

D0008A

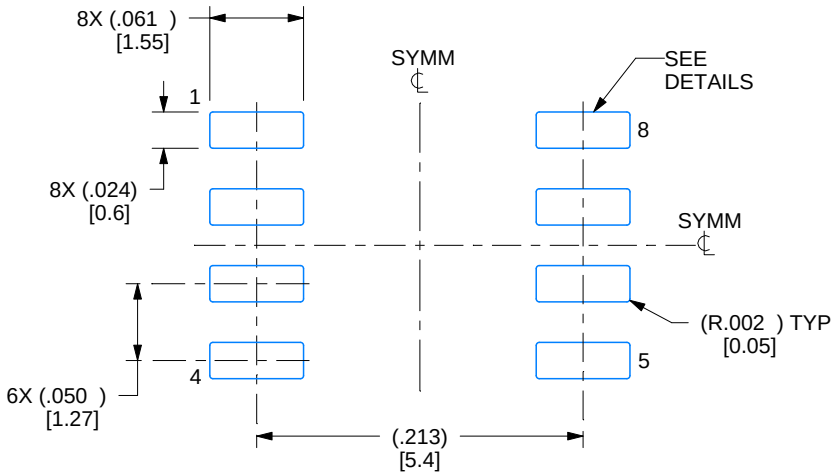
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

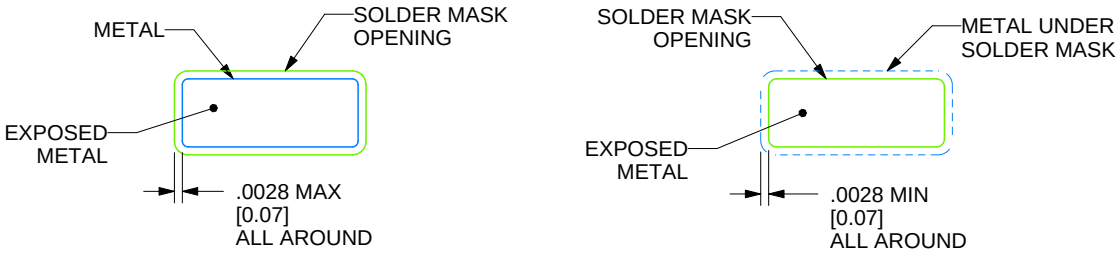


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

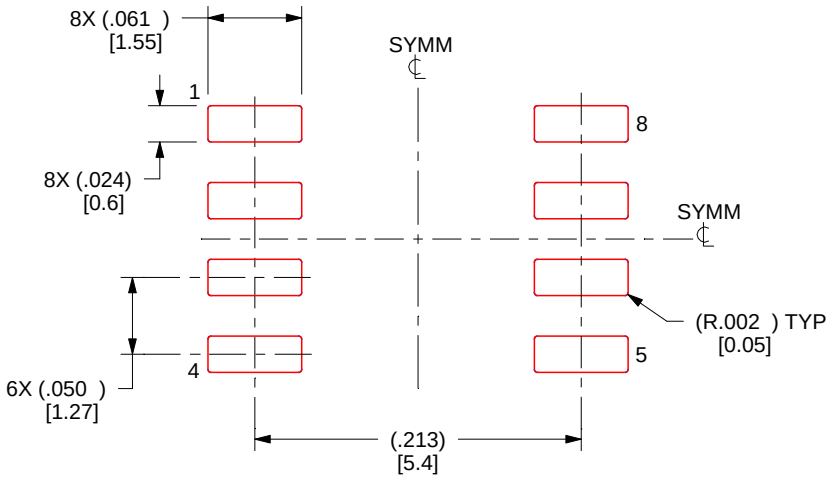
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265