74HC4052; 74HCT4052

Dual 4-channel analog multiplexer/demultiplexer

Rev. 15 — 21 March 2024 Product data sheet

1. General description

The 74HC4052; 74HCT4052 is a dual single-pole quad-throw analog switch (2 × SP4T) suitable for use in analog or digital 4:1 multiplexer/demultiplexer applications. Each switch features four independent inputs/outputs (nY0, nY1, nY2 and nY3) and a common input/output (nZ). A digital enable input ($\overline{E}$) and two digital select inputs (S0 and S1) are common to both switches. When $\overline{E}$ is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide analog input voltage range from -5 V to +5 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Low ON resistance:
  - 80 Ω (typical) at V_{CC} - V_{EE} = 4.5 V
  - 70 Ω (typical) at V_{CC} - V_{EE} = 6.0 V
  - 60 Ω (typical) at V_{CC} - V_{EE} = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ±5 V analog signals
- Typical 'break before make' built-in
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For 74HC4052: CMOS level
  - For 74HCT4052: TTL level
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

nexperia

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4052D 74HCT4052D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4052PW 74HCT4052PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4052BQ 74HCT4052BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HC4052BZ 74HCT4052BZ	-40 °C to +125 °C	DHXQFN16	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 16 terminals; 0.4 mm pitch; body 2 mm × 2.4 mm × 0.48 mm	SOT8016-1

5. Functional diagram

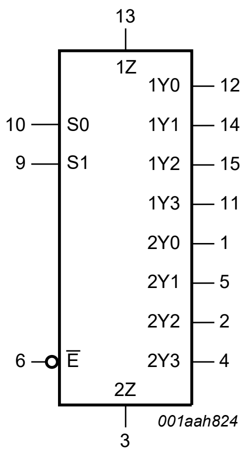


Fig. 1. Logic symbol

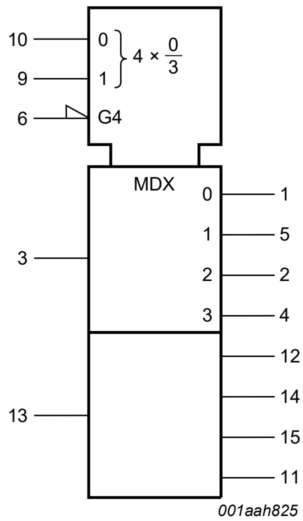


Fig. 2. IEC logic symbol

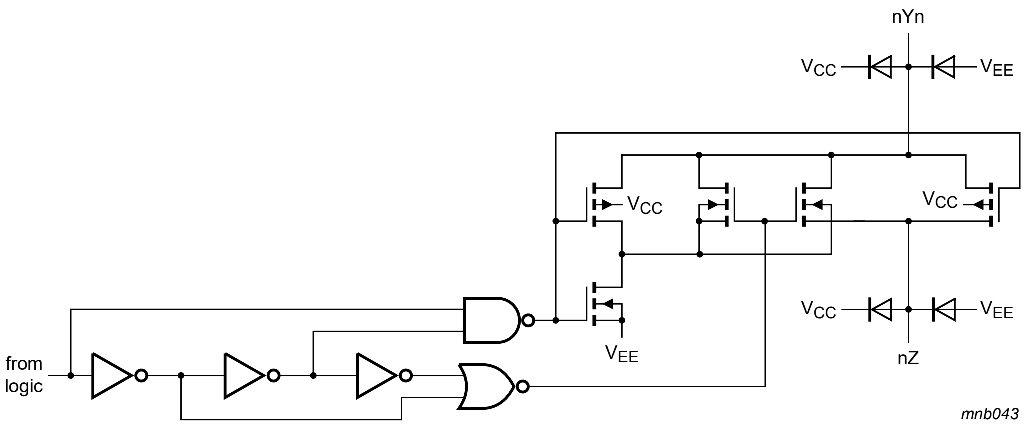


Fig. 3. Schematic diagram (one switch)

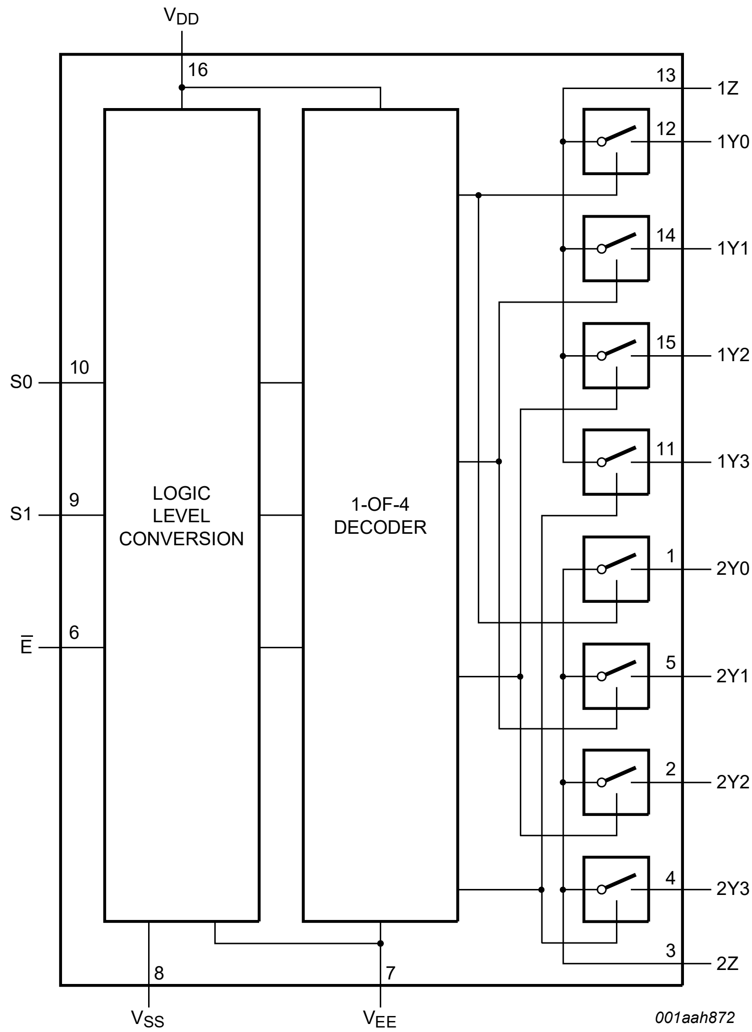
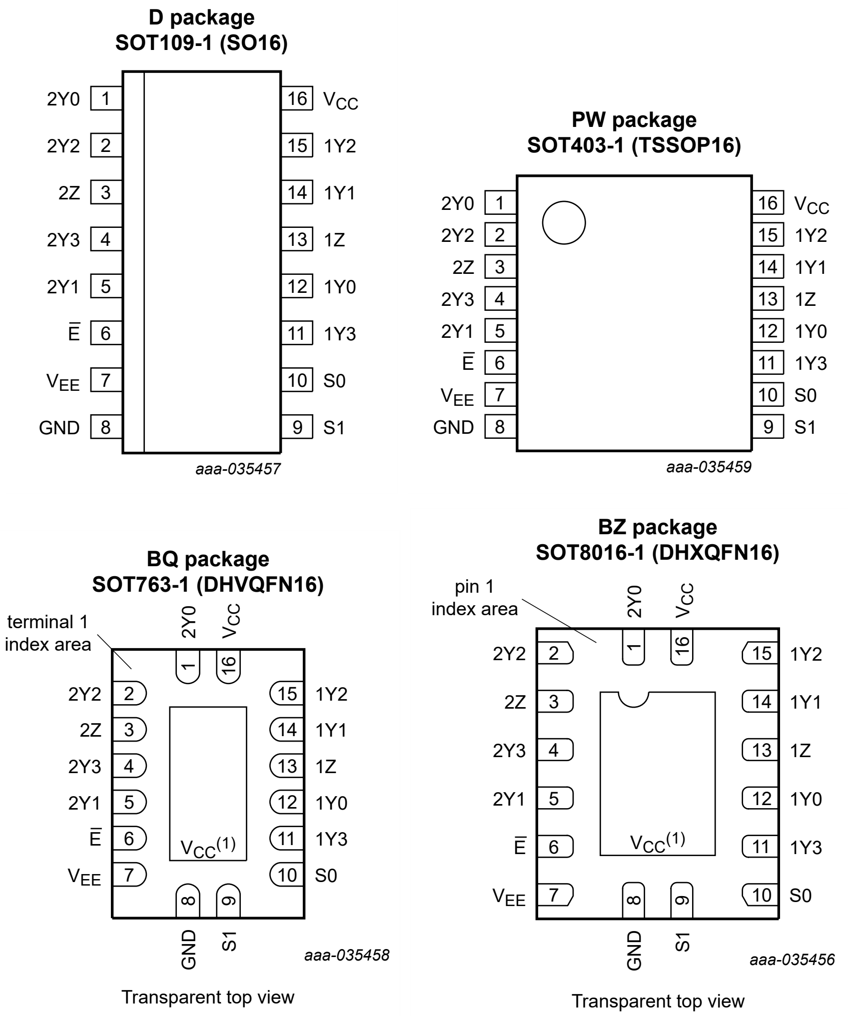


Fig. 4. Functional diagram

6. Pinning information

6.1. Pinning



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0, 2Y1, 2Y2, 2Y3	1, 5, 2, 4	independent input or output
1Z, 2Z	13, 3	common input or output
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	negative supply voltage
GND	8	ground (0 V)
S0, S1	10, 9	select logic input
1Y0, 1Y1, 1Y2, 1Y3	12, 14, 15, 11	independent input or output
V_{CC}	16	positive supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input			Channel on
$\overline{E}$	**S1**	**S0**	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages are referenced to V_{EE} = GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	[1]	-0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V	-	±20	mA
I_{SW}	switch current	-0.5 V $< V_{SW} < V_{CC} + 0.5$ V	-	±25	mA
I_{EE}	supply current		-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-	-50	mA
T_{stg}	storage temperature		-65	+150	°C
P	power dissipation	per switch	-	100	mW
P_{tot}	total power dissipation	SOT109-1; SOT403-1; SOT763-1 [2]	-	500	mW
		SOT8016-1	-	250	mW

[1] To avoid drawing V_{CC} current out of pins nZ, when switch current flows in pins nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pins nZ, no V_{CC} current will flow out of pins nYn. In this case there is no limit for the voltage drop across the switch, but the voltages at pins nYn and nZ may not exceed V_{CC} or V_{EE}.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4052			74HCT4052			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage	see Fig. 5 and Fig. 6							
		V_{CC} - GND	2.0	5.0	10.0	4.5	5.0	5.5	V
		$V_{CC} - V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	GND	-	V_{CC}	V
V_{SW}	switch voltage		V_{EE}	-	V_{CC}	V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
		V_{CC} = 10.0 V	-	-	31	-	-	-	ns/V

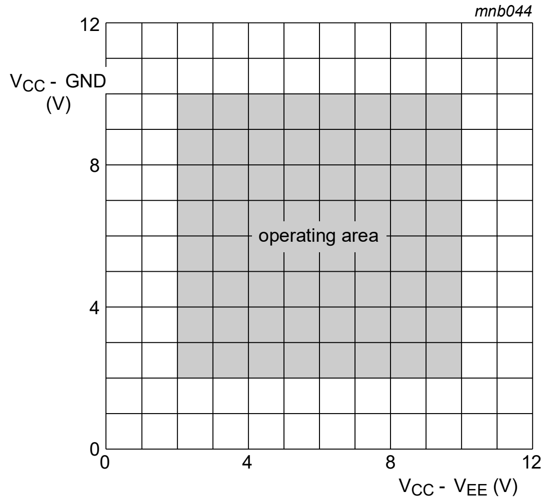


Fig. 5. Guaranteed operating area as a function of the supply voltages for 74HC4052

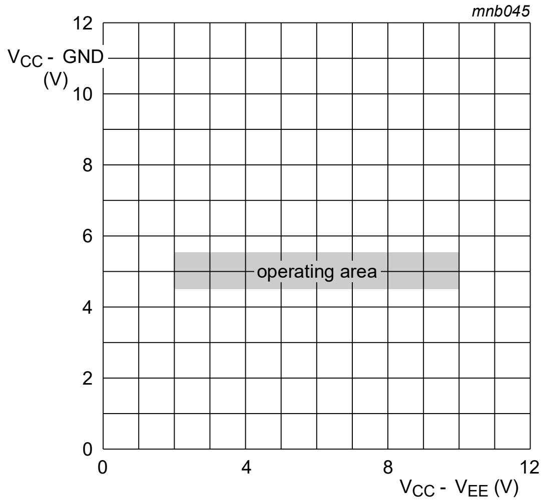


Fig. 6. Guaranteed operating area as a function of the supply voltages for 74HCT4052

10. Static characteristics

Table 6. R_{ON} resistance per switch for 74HC4052 and 74HCT4052

$V_I = V_{IH}$ or V_{IL}; for test circuit see Fig. 7.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

For 74HC4052: V_{CC} - GND or V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

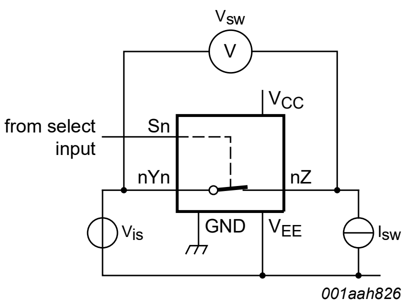
For 74HCT4052: V_{CC} - GND = 4.5 V and 5.5 V, V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C							
$R_{ON(peak)}$	ON resistance (peak)	V_{is} = V_{CC} to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	100	225	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	90	200	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA		-	70	165	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_{is} = V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	150	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	80	175	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	70	150	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA		-	60	130	Ω
		V_{is} = V_{CC}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	150	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	90	200	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	80	175	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA		-	65	150	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_{is} = V_{CC} to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	9	-	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V		-	8	-	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	6	-	Ω

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +125 °C							
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to V_{EE}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	270	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	240	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA		-	-	195	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	210	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	180	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA		-	-	160	Ω
		$V_{is} = V_{CC}$					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	[2]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	240	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA		-	-	210	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA		-	-	180	Ω

[1] All typical values are measured at T_{amb} = 25 °C.

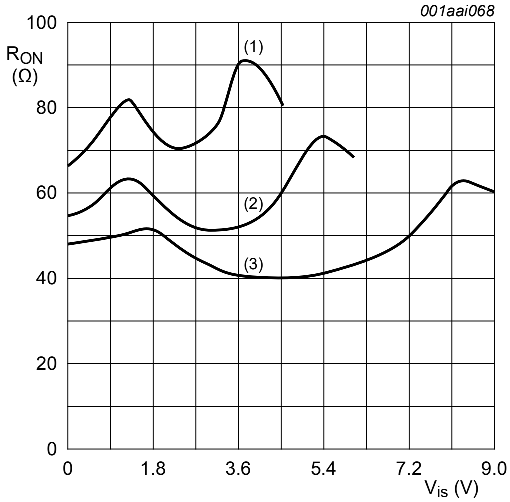
[2] When supply voltages ($V_{CC} - V_{EE}$) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.



V_{is} = 0 V to ($V_{CC} - V_{EE}$).

$$R_{ON} = \frac{V_{sw}}{I_{sw}}$$

Fig. 7. Test circuit for measuring R_{ON}



V_{is} = 0 V to ($V_{CC} - V_{EE}$).

(1) V_{CC} = 4.5 V

(2) V_{CC} = 6 V

(3) V_{CC} = 9 V

Fig. 8. Typical R_{ON} as a function of input voltage V_{is}

Table 7. Static characteristics for 74HC4052

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
		V_{CC} = 9.0 V	6.3	4.7	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
		V_{CC} = 9.0 V	-	4.3	2.7	V
I_I	input leakage current	V_{EE} = 0 V; V_I = V_{CC} or GND				
		V_{CC} = 6.0 V	-	-	±1.0	μA
		V_{CC} = 10.0 V	-	-	±2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 9				
		per channel	-	-	±1.0	μA
		all channels	-	-	±2.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 10	-	-	±2.0	μA
I_{CC}	supply current	V_{EE} = 0 V; V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 6.0 V	-	-	80.0	μA
		V_{CC} = 10.0 V	-	-	160.0	μA
C_I	input capacitance		-	3.5	-	pF
C_{sw}	switch capacitance	independent pins nYn	-	5	-	pF
		common pins nZ	-	12	-	pF
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
		V_{CC} = 9.0 V	6.3	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
		V_{CC} = 9.0 V	-	-	2.7	V
I_I	input leakage current	V_{EE} = 0 V; V_I = V_{CC} or GND				
		V_{CC} = 6.0 V	-	-	±1.0	μA
		V_{CC} = 10.0 V	-	-	±2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 9				
		per channel	-	-	±1.0	μA
		all channels	-	-	±2.0	μA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 10	-	-	±2.0	μA
I_{CC}	supply current	V_{EE} = 0 V; V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 6.0 V	-	-	160.0	μA
		V_{CC} = 10.0 V	-	-	320.0	μA

[1] All typical values are measured at T_{amb} = 25 °C.

Table 8. Static characteristics for 74HCT4052

Voltages are referenced to GND (ground = 0 V).

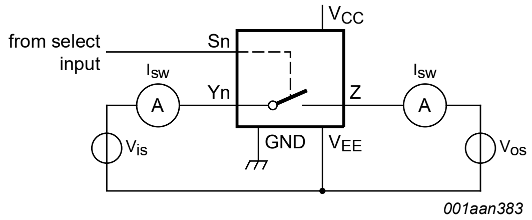
V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 9				
		per channel	-	-	±1.0	μA
		all channels	-	-	±2.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 10	-	-	±2.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	80.0	μA
		V_{CC} = 5.0 V; V_{EE} = -5.0 V	-	-	160.0	μA
ΔI_{CC}	additional supply current	per input; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V	-	45	202.5	μA
C_I	input capacitance		-	3.5	-	pF
C_{sw}	switch capacitance	independent pins nYn	-	5	-	pF
		common pins nZ	-	12	-	pF
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 9				
		per channel	-	-	±1.0	μA
		all channels	-	-	±2.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 10	-	-	±2.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	160.0	μA
		V_{CC} = 5.0 V; V_{EE} = -5.0 V	-	-	320.0	μA

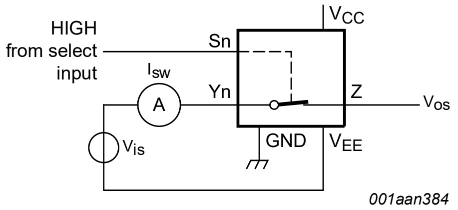
Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V	-	-	220.5	μA

[1] All typical values are measured at T_{amb} = 25 °C.



$V_{is} = V_{CC}$ and $V_{os} = V_{EE}$.
$V_{is} = V_{EE}$ and $V_{os} = V_{CC}$.

Fig. 9. Test circuit for measuring OFF-state current



$V_{is} = V_{CC}$ and V_{os} = open-circuit.
$V_{is} = V_{EE}$ and V_{os} = open-circuit.

Fig. 10. Test circuit for measuring ON-state current

11. Dynamic characteristics

Table 9. Dynamic characteristics for 74HC4052

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; for test circuit see Fig. 13.
V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
t_{pd}	propagation delay	V_{is} to V_{os}; $R_L = \infty$ Ω; see Fig. 11 [2]				
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	14	75	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	5	15	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	4	13	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	4	10	ns
t_{on}	turn-on time	$\overline{E}$, Sn to V_{os}; $R_L = \infty$ Ω; see Fig. 12 [3]				
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	105	405	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	38	81	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF	-	28	-	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	30	69	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	26	58	ns

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{off}	turn-off time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Fig. 12	[4]				
		V_{CC} = 2.0 V; V_{EE} = 0 V		-	74	315	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	27	63	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		-	21	-	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		-	22	54	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	22	48	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to V_{CC}	[5]	-	57	-	pF
T_{amb} = -40 °C to +125 °C							
t_{pd}	propagation delay	V_{is} to V_{os}; R_L = ∞ Ω; see Fig. 11	[2]				
		V_{CC} = 2.0 V; V_{EE} = 0 V		-	-	90	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	18	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		-	-	15	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	-	12	ns
t_{on}	turn-on time	$\overline{E}$, Sn to V_{os}; R_L = ∞ Ω; see Fig. 12	[3]				
		V_{CC} = 2.0 V; V_{EE} = 0 V		-	-	490	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	98	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		-	-	83	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	-	69	ns
t_{off}	turn-off time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Fig. 12	[4]				
		V_{CC} = 2.0 V; V_{EE} = 0 V		-	-	375	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	75	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		-	-	64	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	-	57	ns

[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_{on} is the same as t_{PZH} and t_{PZL}.
[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
N = number of inputs switching;
$\Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
C_L = output load capacitance in pF;
C_{sw} = switch capacitance in pF;
V_{CC} = supply voltage in V.

Table 10. Dynamic characteristics for 74HCT4052

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; for test circuit see Fig. 13.
V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C							
t_{pd}	propagation delay	V_{is} to V_{os}; R_L = ∞ Ω; see Fig. 11	[2]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	5	15	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	4	10	ns
t_{on}	turn-on time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Fig. 12	[3]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	41	88	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		-	18	-	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	28	60	ns
t_{off}	turn-off time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Fig. 12	[4]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	26	63	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		-	13	-	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	21	48	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to V_{CC} - 1.5 V	[5]	-	57	-	pF
T_{amb} = -40 °C to +125 °C							
t_{pd}	propagation delay	V_{is} to V_{os}; R_L = ∞ Ω; see Fig. 11	[2]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	18	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	-	12	ns
t_{on}	turn-on time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Fig. 12	[3]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	105	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	-	72	ns
t_{off}	turn-off time	$\overline{E}$, Sn to V_{os}; R_L = 1 kΩ; see Fig. 12	[4]				
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	-	75	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	-	57	ns

[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_{on} is the same as t_{PZH} and t_{PZL}.
[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma\{(C_L + C_{sw}) \times V_{CC}{}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
N = number of inputs switching;
$\Sigma\{(C_L + C_{sw}) \times V_{CC}{}^2 \times f_o\}$ = sum of outputs;
C_L = output load capacitance in pF;
C_{sw} = switch capacitance in pF;
V_{CC} = supply voltage in V.

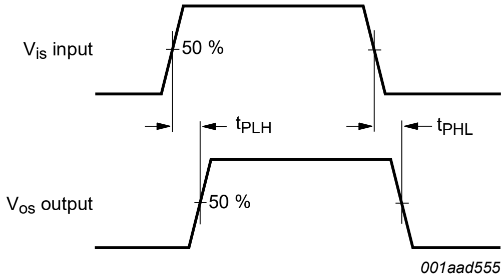
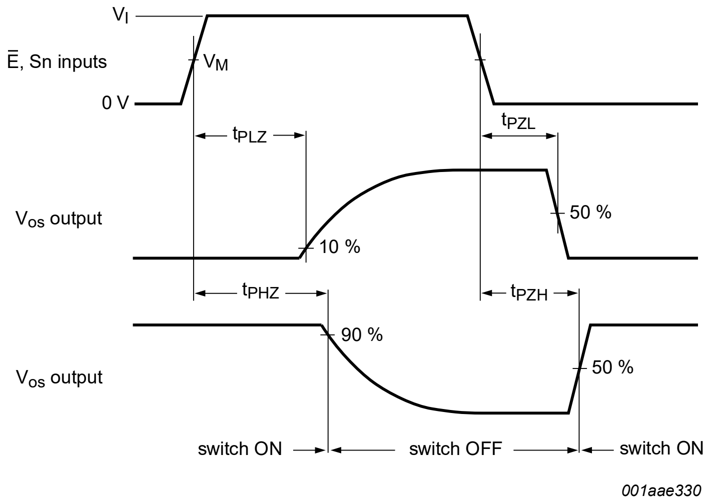


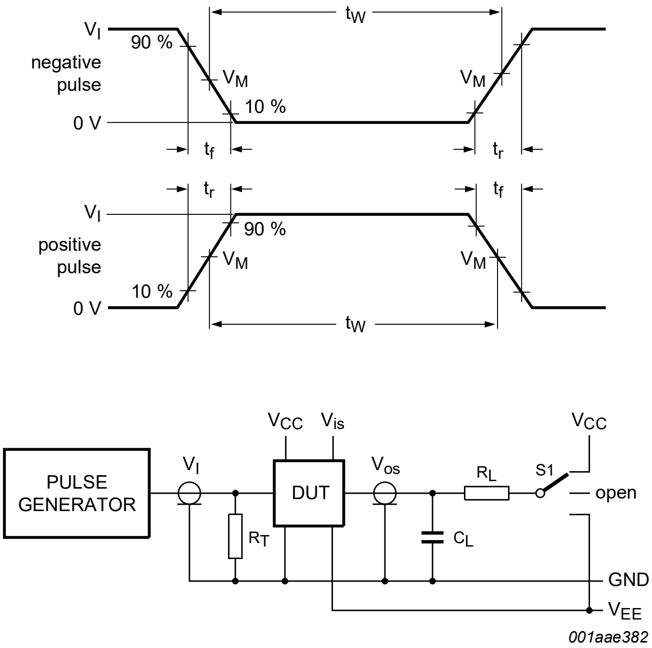
Fig. 11. Input (V_{is}) to output (V_{os}) propagation delays



For 74HC4052: $V_M = 0.5 \times V_{CC}$.

For 74HCT4052: $V_M = 1.3$ V.

Fig. 12. Turn-on and turn-off times



Definitions for test circuit; see Table 11:

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

Fig. 13. Test circuit for measuring switching times

Table 11. Test data

Test	Input				Load		S1 position
	V_I [1]	V_{is}	t_r, t_f		C_L	R_L	
			at f_{max}	other [2]			
t_{PHL}, t_{PLH}	V_{CC}	pulse	< 2 ns	6 ns	50 pF	1 kΩ	open
t_{PZH}, t_{PHZ}	V_{CC}	V_{CC}	< 2 ns	6 ns	50 pF	1 kΩ	V_{EE}
t_{PZL}, t_{PLZ}	V_{CC}	V_{EE}	< 2 ns	6 ns	50 pF	1 kΩ	V_{CC}

[1] For 74HCT4052: V_I = 3 V

[2] t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

11.1. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C; C_L = 50 pF.
V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.
V_{os} is the output voltage at pins nYn or nZ, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
d_{sin}	sine-wave distortion	f_i = 1 kHz; R_L = 10 kΩ; see Fig. 14					
		V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = -2.25 V		-	0.04	-	%
		V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	0.02	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see Fig. 14					
		V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = -2.25 V		-	0.12	-	%
		V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	0.06	-	%
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; f_i = 1 MHz; see Fig. 15					
		V_{CC} = 2.25 V; V_{EE} = -2.25 V	[1]	-	-50	-	dB
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	[1]	-	-50	-	dB
Xtalk	crosstalk	between two switches/multiplexers; R_L = 600 Ω; f_i = 1 MHz; see Fig. 16					
		V_{CC} = 2.25 V; V_{EE} = -2.25 V	[1]	-	-60	-	dB
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	[1]	-	-60	-	dB
V_{ct}	crosstalk voltage	peak-to-peak value; between control and any switch; R_L = 600 Ω; f_i = 1 MHz; $\overline{E}$ or Sn square wave between V_{CC} and GND; t_r = t_f = 6 ns; see Fig. 17					
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	110	-	mV
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		-	220	-	mV
$f_{(-3dB)}$	-3 dB frequency response	R_L = 50 Ω; see Fig. 18					
		V_{CC} = 2.25 V; V_{EE} = -2.25 V	[2]	-	170	-	MHz
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	[2]	-	180	-	MHz

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

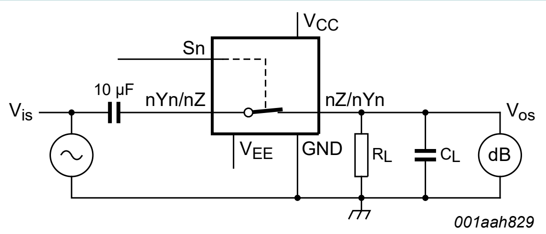
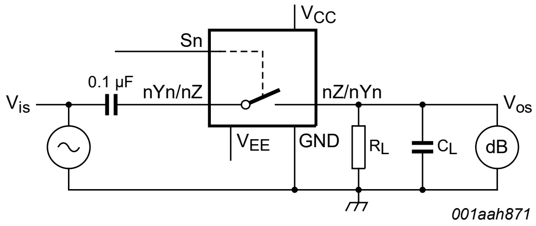
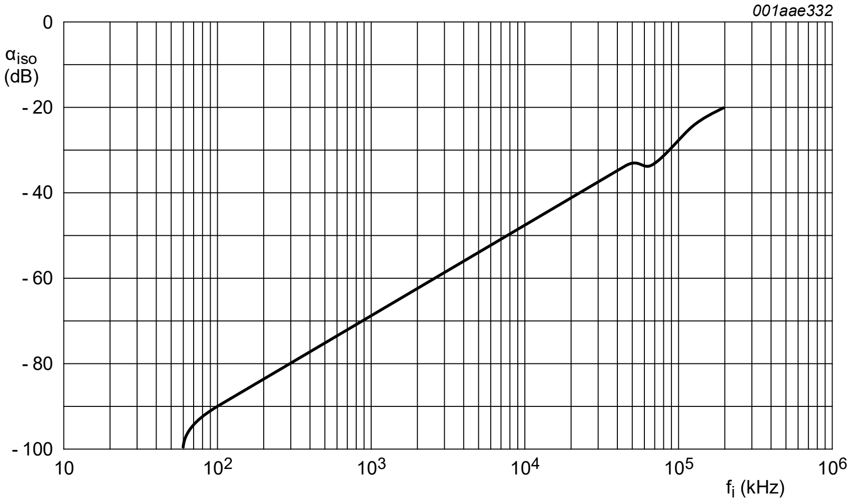


Fig. 14. Test circuit for measuring sine-wave distortion



V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 600 Ω; R_S = 1 kΩ.

a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Fig. 15. Test circuit for measuring isolation (OFF-state)

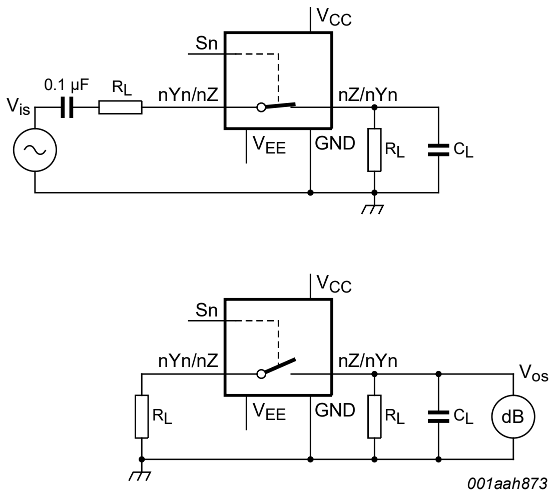


Fig. 16. Test circuits for measuring crosstalk between any two switches/multiplexers

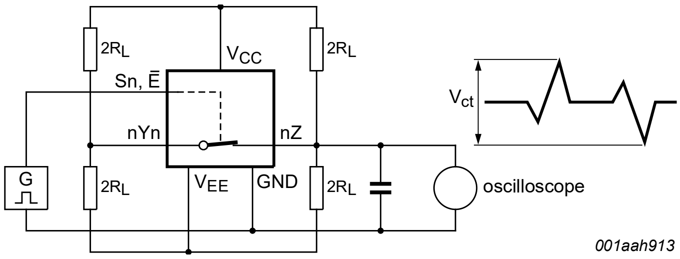
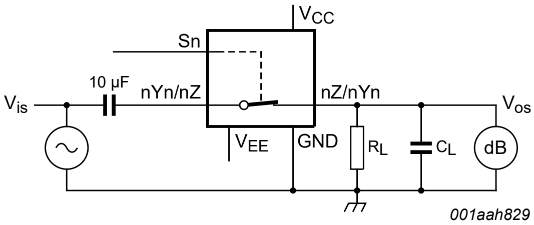
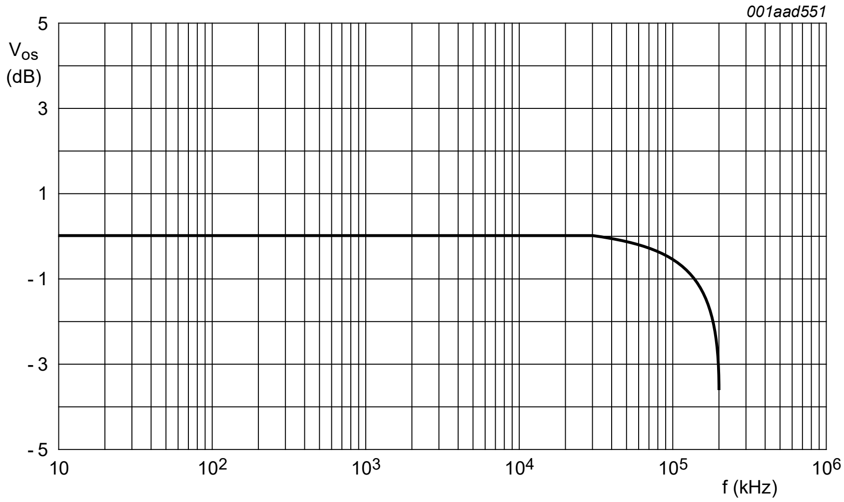


Fig. 17. Test circuit for measuring crosstalk between control input and any switch



V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 50 Ω; R_S = 1 kΩ.

a. Test circuit

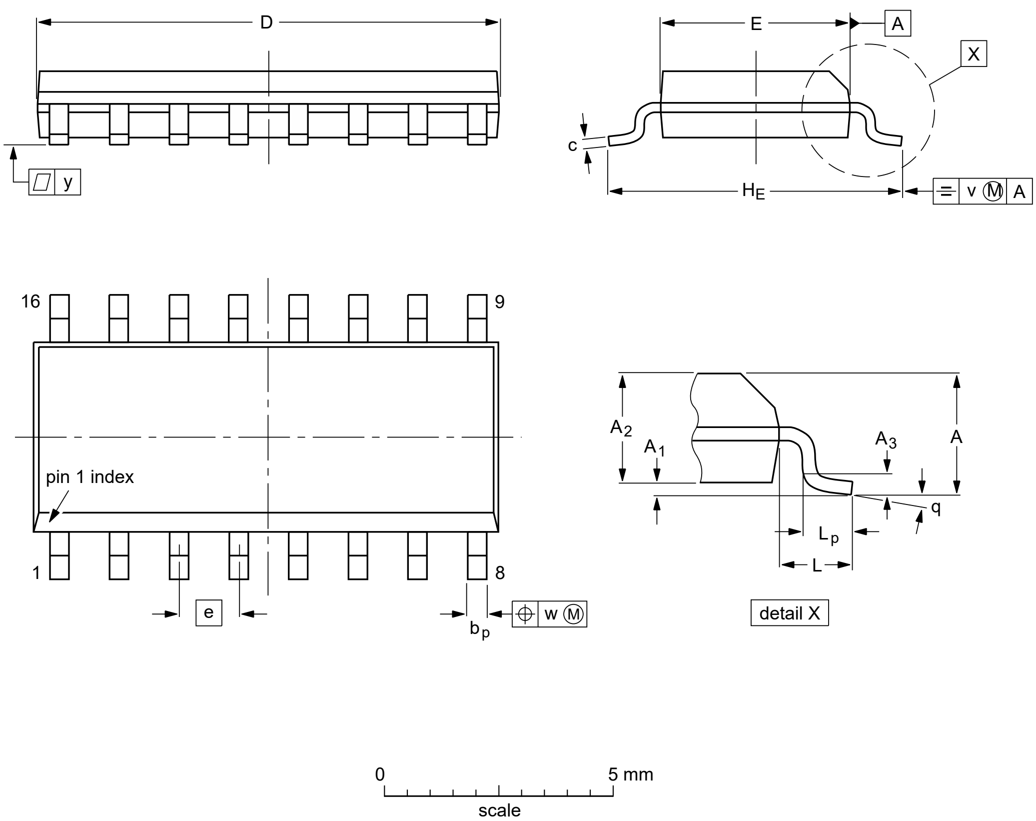


b. Typical frequency response

Fig. 18. Test circuit for frequency response

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

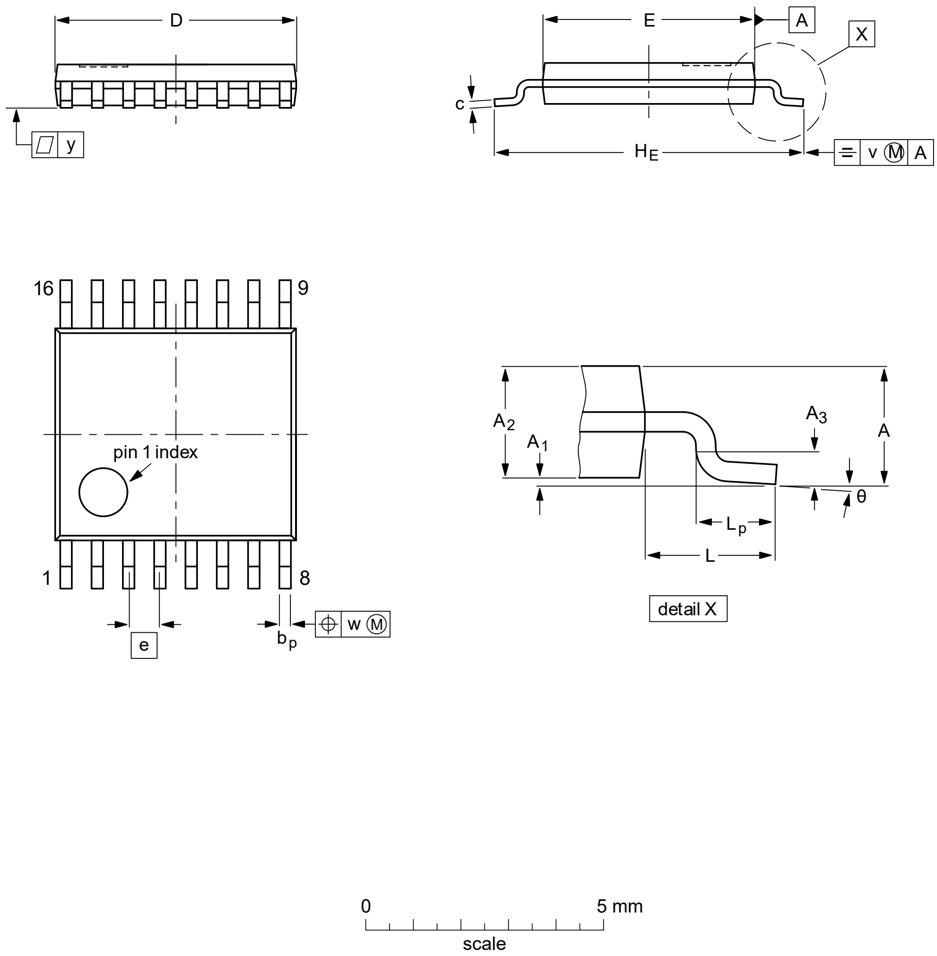
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 19. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

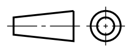
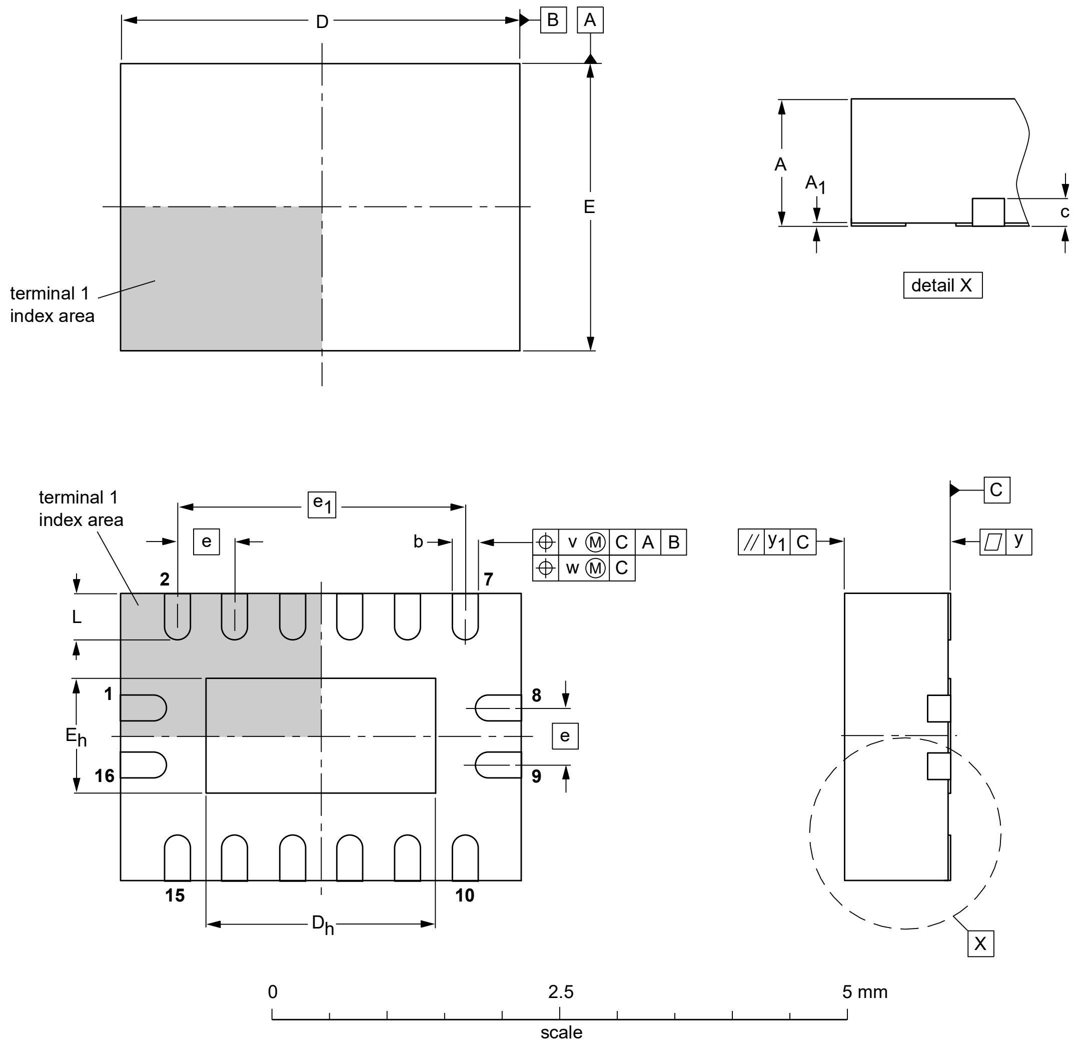
Outline version	References IEC	References JEDEC	References JEITA		European projection	Issue date
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 20. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

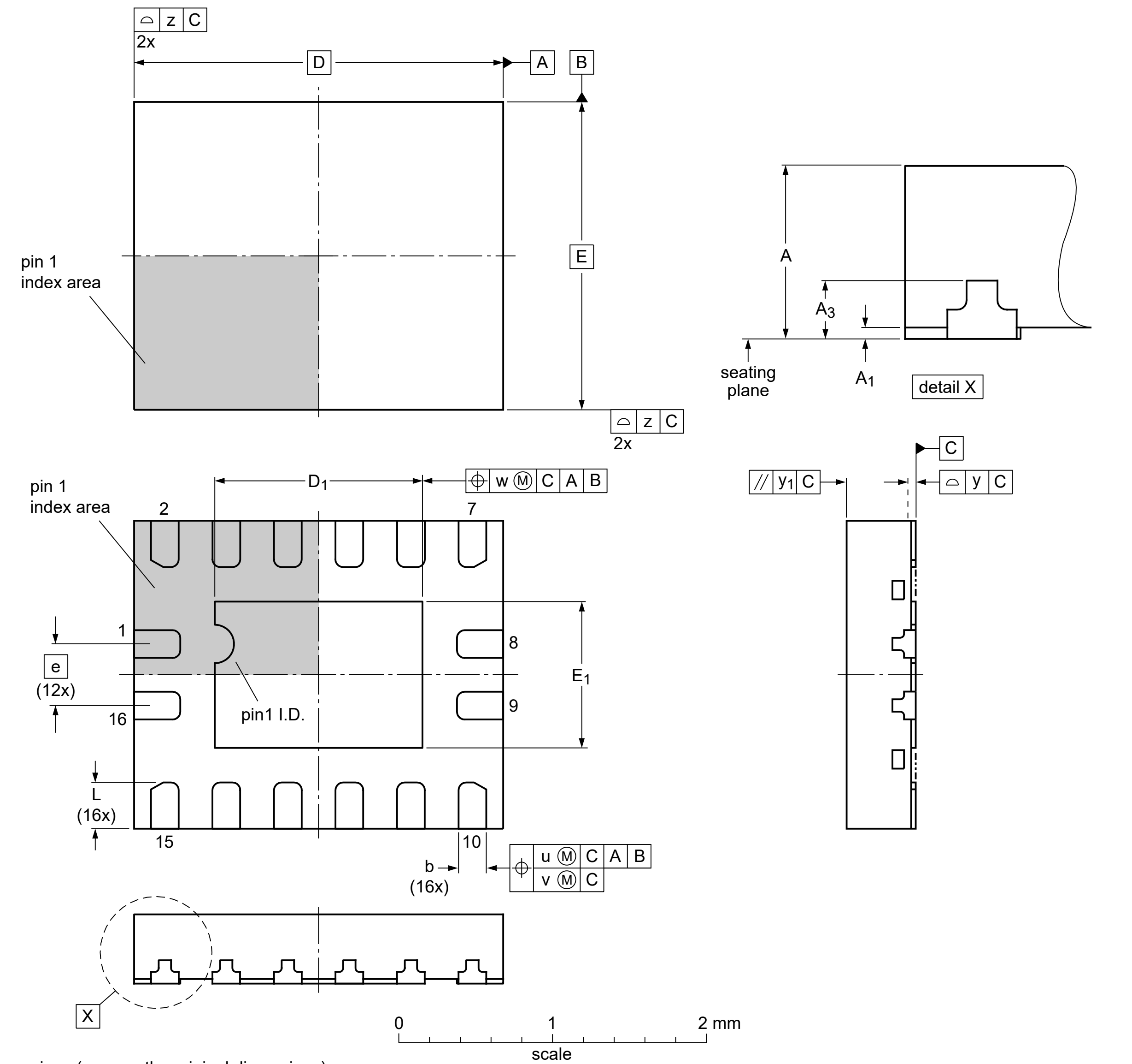
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 21. Package outline SOT763-1 (DHVQFN16)

DHXQFN16: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 16 terminals; 0.4 mm pitch; body 2 mm x 2.4 mm x 0.48 mm **SOT8016-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_3	b	D	D_1	E	E_1	e	k	L	u	v	w	y	y_1	z
mm	max	0.48	0.05	0.15 (typ)	0.23		1.40		1.00			0.35						
	nom	0.45	0.02		0.18	2.4	1.35	2.0	0.95	0.4		0.30	0.1	0.05	0.1	0.05	0.05	0.05
	min	0.42	0.00		0.13		1.30		0.90		0.2	0.25						

sot8016-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8016-1						~~20-09-18~~ 20-09-22

Fig. 22. Package outline SOT8016-1 (DHXQFN16)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4052 v.15	20240321	Product data sheet	-	74HC_HCT4052 v.14
Modifications:	• Fig. 19, Fig. 20: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT4052 v.14	20230209	Product data sheet	-	74HC_HCT4052 v.13
Modifications:	• Type numbers 74HC4052BZ and 74HCT4052BZ (SOT8016-1/DXQFN16) added.			
74HC_HCT4052 v.13	20171010	Product data sheet	-	74HC_HCT4052 v.12
Modifications:	• Type numbers 74HC4052DB and 74HCT4052DB (SOT338-1/SSOP16) removed. • Section 2 updated. • Section 8: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT4052 v.12	20171010	Product data sheet	-	74HC_HCT4052 v.11
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT4052 v.11	20160210	Product data sheet	-	74HC_HCT4052 v.10
Modifications:	• Type numbers 74HC4052N and 74HCT4052N (SOT38-4) removed.			
74HC_HCT4052 v.10	20120719	Product data sheet	-	74HC_HCT4052 v.9
Modifications:	• CDM added to features.			
74HC_HCT4052 v.9	20111213	Product data sheet	-	74HC_HCT4052 v.8
Modifications:	• Legal pages updated.			
74HC_HCT4052 v.8	20110511	Product data sheet	-	74HC_HCT4052 v.7
74HC_HCT4052 v.7	20110112	Product data sheet	-	74HC_HCT4052 v.6
74HC_HCT4052 v.6	20100111	Product data sheet	-	74HC_HCT4052 v.5
74HC_HCT4052 v.5	20080505	Product data sheet	-	74HC_HCT4052 v.4
74HC_HCT4052 v.4	20041111	Product specification	-	74HC_HCT4052 v.3
74HC_HCT4052 v.3	20030516	Product specification	-	74HC_HCT4052 v.2
74HC_HCT4052 v.2	19901201	-	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 21 March 2024