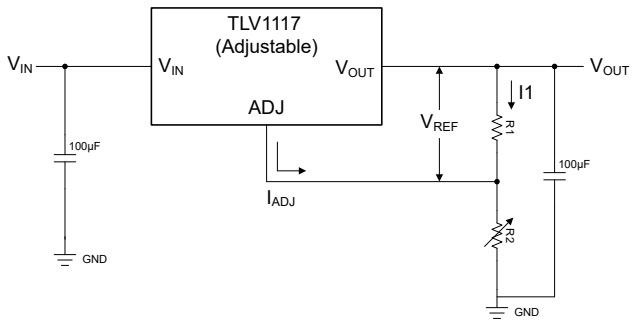
TLV1117 15V, 800mA, Adjustable and Fixed Linear Voltage Regulator

1 Features

- Input voltage range V_{IN}: 2.7V to 15V
- Output voltage options:
  - Fixed: 1.5V to 5V
  - Adjustable: 1.25V to 13.8V
- Output current: 800mA
- Output accuracy (new chip):
  - Fixed: ±1.0% at T_J = 25°C
  - Adjustable: ±1.0% at T_J = 25°C
- Quiescent current (I_Q):
  - Fixed: 60µA (typical, approximately 1.5µA in shutdown) (new chip)
  - Adjustable: 5mA (typical)
- Packages:
  - New chip:
    - 4-pin SOT-223 (DCY), $R_{\theta JA}$ = 95.4°C/W
    - 3-pin, TO-252 (KVU), $R_{\theta JA}$ = 67.2°C/W
  - Legacy chip:
    - 3-pin, TO-263 (KTT), $R_{\theta JA}$ = 27.5°C/W
    - 3-pin, TO-220 (KCT, KCS), $R_{\theta JA}$ = 30.1°C/W
    - 8-pin, WSON (DRJ), $R_{\theta JA}$ = 38.3°C/W

2 Applications

- Appliances
- Home theater and entertainment
- Motor drives
- HVAC and building security systems
- Smart meters



Simplified Application Schematic for the Adjustable Regulator

3 Description

The TLV1117 is a linear voltage that provides up to 800mA of output current with a supported input voltage range from 2.7V to 15V. The fixed version of the TLV1117 supports an output range from 1.5V to 5V and the adjustable version supports an output range from 1.25V to 13.8V. This range is designed for a wide variety of applications.

For the adjustable version, use a minimum 1.7mA (typical) load current for stable operation. Place a minimum 10µF tantalum capacitor at the output to improve the transient response and stability.

For the fixed version (new chip), there is no minimum load current requirement on the voltage regulator output. The fixed version of the TLV1117 (new chip), has an internal soft-start feature to reduce inrush current during start-up. This feature helps save space and cost in a design by minimizing input capacitance. The fixed version (new chip) also features a foldback current limit that limits device power dissipation during high-load current faults or shorting events.

Package Information

PART NUMBER	PACKAGE(1) (2)	PACKAGE SIZE(3)
TLV1117	**New Chip**	
	DCY (SOT-223, 4)	6.5mm × 7mm
	KVU (TO-252, 3)	6.6mm × 10.11mm
	NDP (TO-252, 3)	6.58mm × 9.92mm
	Legacy Chip	
	DRJ (WSON, 8)	4mm × 4mm
	KCS (TO-220, 3)	10.16mm × 28.65mm
	KCT (TO-220, 3)	10.16mm × 28.65mm
	KTT (DDPAK/TO-263, 3)	10.18mm × 15.24mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) For legacy and new chip details, see the *Device Nomenclature* section.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....5
5.4 Thermal Information (Legacy Chip)....6
5.5 Thermal Information (New Chip)....6
5.6 Electrical Characteristics....7
5.7 Typical Characteristics....10
6 Detailed Description....17
6.1 Overview....17
6.2 Functional Block Diagrams....17
6.3 Feature Description....18
6.4 Device Functional Modes....21
7 Application and Implementation....23
7.1 Application Information....23
7.2 Typical Application (Adjustable Output)....25
7.3 Power Supply Recommendations....28
7.4 Layout....28
8 Device and Documentation Support....29
8.1 Device Support....29
8.2 Receiving Notification of Documentation Updates....29
8.3 Support Resources....29
8.4 Trademarks....29
8.5 Electrostatic Discharge Caution....29
8.6 Glossary....29
9 Revision History....30
10 Mechanical, Packaging, and Orderable Information....30

4 Pin Configuration and Functions

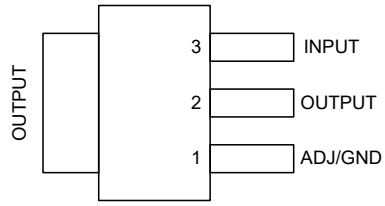


Figure 4-1. DCY Package, 4-Pin SOT (Top View)

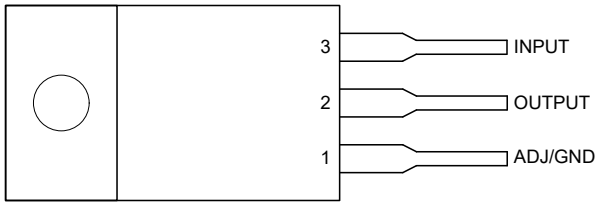


Figure 4-2. KCT and KCS Package, 3-Pin TO-220 (Top View)

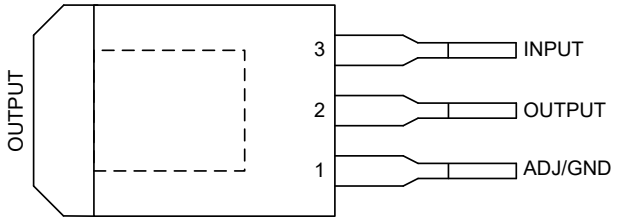


Figure 4-3. KTT Package, 3-Pin TO-263 (Top View)

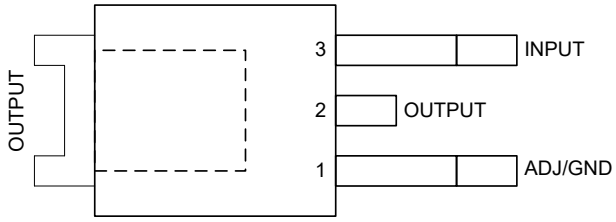


Figure 4-4. KVU Package, 3-Pin TO-252 (Top View)

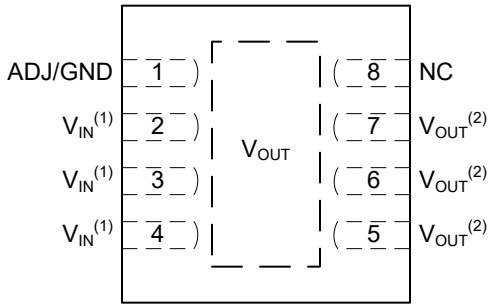


Figure 4-5. DRJ Package, 8-Pin WSON (Top View)

Table 4-1. Pin Functions

PIN						TYPE	DESCRIPTION
NAME	KTT	KVU	DCY	DRJ	KCT		
ADJ/GND	1	1	1	1	1	I/O	Adjust pin for adjustable output option. Ground pin for fixed output option.
INPUT (V_{IN})	3	3	3	2, 3, 4	3	I	Input voltage pin for the regulator. For the DRJ package, connect the V_{IN} and V_{OUT} pins together.
OUTPUT (V_{OUT})	2	2	2	5, 6, 7	2	O	Output voltage pin for the regulator. For the DRJ package, connect the V_{IN} and V_{OUT} pins together.
NC	—	—	—	8	—	—	No connect.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN} (2)	Continuous input voltage (legacy chip)		16	V
	Continuous input voltage (new chip)	–0.3	20	
V_{OUT} (3)	Output voltage (new chip, fixed version only)	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current (new chip, fixed version only)	Internally limited		A
Power	Power dissipation	Package limited (4)		W
Temperature	Operating junction (T_j)	–50	150	°C
	Storage (T_{stg})	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings,* the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages with respect to GND.
(3) V_{IN} + 0.3V or 20V (whichever is smaller).
(4) See *Thermal Information* table for further details.

5.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip, Fixed Output)	VALUE (New Chip, Adjustable Output)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	±3000	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	±1000	NA	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage (legacy chip)	TLV1117	2.7		15	V
		TLV1117-15	2.9		15	
		TLV1117-18	3.2		15	
		TLV1117-25	3.9		15	
		TLV1117-33	4.7		15	
		TLV1117-50	6.4		15	
	Input voltage (new chip, fixed output)		2.5		18	
	Input voltage (new chip, adjustable output)				15	
V_{OUT}	Output voltage (new chip, fixed output)		0.8		13.5	V
	Output voltage (new chip, adjustable output)				13.8	
I_{OUT}	Output current (legacy chip)				0.8	A
	Output current (new chip, fixed output)	$2.5V \le V_{IN} \le 3V$	0		0.8	
		$V_{IN} \ge 3V$	0		1	
	Output current (new chip, adjustable output)				0.8	
C_{OUT} ESR	Output capacitor ESR (new chip, fixed output)		2		500	mΩ
C_{OUT}	Output capacitor (new chip, fixed output)(1)		1	2.2	220	µF
C_{IN}	Input capacitor (new chip, fixed output)(2)			1		
T_J (3)	Junction temperature (legacy chip)	TLV1117C	0		125	°C
		TLV1117I	–40		125	
	Junction temperature (new chip, fixed output)	TLV1117C/I	–40		125	
	Junction temperature (new chip, adjustable output)	TLV1117C	0		125	
		TLV1117I	–40		125	

(1) Effective output capacitance of 0.47µF minimum required for stability.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(3) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

5.4 Thermal Information (Legacy Chip)

THERMAL METRIC[1]		Legacy chip [2]							UNIT
		KTE (PowerFlex)	KTP (PowerFlex)	DRJ	DCY	KVU	KCS, KCT	KTT	
		3 PINS	3 PINS	8 PINS	4 PINS	3 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.6	49.2	38.3	104.3	50.9	30.1	27.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.7	60.6	36.5	53.7	57.9	44.6	43.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.2	3.1	60.5	5.7	34.8	1.2	17.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.9	8.7	0.2	3.1	6	5	2.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	3.1	3	12	5.5	23.7	1.2	9.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3	3	4.7	n/a	0.4	0.4	0.3	°C/W
$R_{\theta JP}$	Thermal resistance between the die junction and the bottom of the exposed pad.	2.7	1.4	1.78	n/a	n/a	3	1.94	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

5.5 Thermal Information (New Chip)

THERMAL METRIC [1]		Fixed Output		Adjustable Output		UNIT
		DCY (SOT–223)	KVU (TO-252)	DCY (SOT–223)	KVU (TO–252)	
		4 PINS	4 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.4	67.2	61.6	45.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.6	71.8	42.5	52.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.7	45.5	10.4	29.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.9	31.6	2.9	4.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.4	45.4	10.3	29.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	40.5	N/A	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.6 Electrical Characteristics

specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.5V or V_{IN} = 2.5V (whichever is greater), I_{OUT} = 10mA, C_{IN} = 1.0µF and C_{OUT} = 1.0µF (unless otherwise noted); typical values are at T_J= 25°C.

PARAMETER		TEST CONDITIONS[1]		MIN [4]	TYP [5]	MAX [4]	UNIT
V_{REF}	Reference voltage (legacy chip)	V_{IN} – V_{OUT} = 2V, I_{OUT} = 10mA, T_J = 25°C	TLV1117x	1.238	1.25	1.262	V
		V_{IN} – V_{OUT} = 1.4V to 10V, I_{OUT} = 10mA to 800mA, 0°C ≤ T_J ≤ 125°C		1.225	1.25	1.27	
		V_{IN} – V_{OUT} = 1.4V to 10V, I_{OUT} = 10mA to 800mA		1.2	1.25	1.29	
	Reference voltage (new chip, adjustable output)	I_{OUT} = 10mA, V_{IN} – V_{OUT} = 2V, T_J = 25°C	TLV1117x	1.238	1.25	1.252	
		10mA ≤ I_{OUT} ≤ 800mA, 1.4V ≤ V_{IN} – V_{OUT} ≤ 10V, T_J = 25°C			1.25		
		10mA ≤ I_{OUT} ≤ 800mA, 1.4V ≤ V_{IN} – V_{OUT} ≤ 10V		1.2		1.29	
V_{OUT}	Output voltage (legacy chip)	V_{IN} = 3.5V, I_{OUT} = 10mA, T_J = 25°C	TLV1117-15	1.485	1.5	1.515	V
		V_{IN} = 2.9V to 10V, I_{OUT} = 0mA to 800mA, 0°C ≤ T_J ≤ 125°C		1.455	1.5	1.545	
		V_{IN} = 2.9V to 10V, I_{OUT} = 0mA to 800mA		1.44	1.5	1.56	
		V_{IN} = 3.8V, I_{OUT} = 10mA, T_J = 25°C	TLV1117-18	1.782	1.8	1.818	
		V_{IN} = 3.2V to 10V, I_{OUT} = 0mA to 800mA, 0°C ≤ T_J ≤ 125°C		1.746	1.8	1.854	
		V_{IN} = 3.2V to 10V, I_{OUT} = 0mA to 800mA		1.728	1.8	1.872	
		V_{IN} = 4.5V, I_{OUT} = 10mA, T_J = 25°C	TLV1117-25	2.475	2.5	2.525	
		V_{IN} = 3.9V to 10V, I_{OUT} = 0mA to 800mA, 0°C ≤ T_J ≤ 125°C		2.450	2.5	2.550	
		V_{IN} = 3.9V to 10V, I_{OUT} = 0mA to 800mA		2.4	2.5	2.525	
		V_{IN} = 5V, I_{OUT} = 10mA, T_J = 25°C	TLV1117-33	3.267	3.3	3.333	
		V_{IN} = 4.75V to 10V, I_{OUT} = 0mA to 800mA, 0°C ≤ T_J ≤ 125°C		3.235	3.3	3.365	
		V_{IN} = 4.75V to 10V, I_{OUT} = 0mA to 800mA		3.168	3.3	3.333	
		V_{IN} = 7V, I_{OUT} = 10mA, T_J = 25°C	TLV1117-50	4.950	5.0	5.050	
		V_{IN} = 6.5V to 12V, I_{OUT} = 0mA to 800mA, 0°C ≤ T_J ≤ 125°C		4.900	5.0	5.1	
		V_{IN} = 6.5V to 12V, I_{OUT} = 0mA to 800mA		4.80	5.0	5.20	
	Output voltage (new chip, fixed output)	I_{OUT} = 10mA, T_J = 25°C		–1		1	%
		VIN ≥ 3.0V, $V_{OUT(NOM)}$ ≤ 9.0V, 1mA ≤ I_{OUT} ≤ 1A		–1.75		1.75	%
		$V_{OUT(NOM)}$ > 9.0V, 1mA ≤ I_{OUT} ≤ 1A		–1.75		1.75	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation (legacy chip)	I_{OUT} = 10mA, V_{IN} – V_{OUT} = 1.5V to 13.75V, 0°C ≤ T_J ≤ 125°C	TLV1117		0.035	0.2	%
		I_{OUT} = 10mA, V_{IN} – V_{OUT} = 1.5V to 13.75V			0.035	0.3	
		I_{OUT} = 0mA, V_{IN} = 2.9V to 10V	TLV1117-15		1	10	mV
		I_{OUT} = 0mA, V_{IN} = 3.2V to 10V	TLV1117-18		1	10	
		I_{OUT} = 0mA, V_{IN} = 3.9V to 10V	TLV1117-25		1	10	
		I_{OUT} = 0mA, V_{IN} = 4.75V to 15V	TLV1117-33		1	10	
		I_{OUT} = 0mA, V_{IN} = 6.5V to 15V	TLV1117-50		1	10	
	Line regulation (new chip, adjustable output)[6]	I_{OUT} = 10mA, 1.5V ≤ V_{IN} – V_{OUT} ≤ 13.75V, T_J = 25°C	TLV1117		0.035		%
		I_{OUT} = 10mA, 1.5V ≤ V_{IN} – V_{OUT} ≤ 13.75V				0.3	%
	Line regulation (new chip, fixed output)[8]	$V_{OUT(NOM)}$ + 1.5V ≤ V_{IN} ≤ 18V, I_{OUT} = 10mA				10	mV

5.6 Electrical Characteristics (continued)

specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.5V or V_{IN} = 2.5V (whichever is greater), I_{OUT} = 10mA, C_{IN} = 1.0µF and C_{OUT} = 1.0µF (unless otherwise noted); typical values are at T_J= 25°C.

PARAMETER		TEST CONDITIONS[1]		MIN [4]	TYP [5]	MAX [4]	UNIT
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation (legacy chip)	I_{OUT} = 0mA to 800mA, V_{IN} = 2.9V, 0°C ≤ T_J ≤ 125°C	TLV1117-15		1	15	mV
		I_{OUT} = 0mA to 800mA, V_{IN} = 3.2V, 0°C ≤ T_J ≤ 125°C	TLV1117-18		1	15	
		I_{OUT} = 0mA to 800mA, V_{IN} = 3.9V, 0°C ≤ T_J ≤ 125°C	TLV1117-25		1	15	
		I_{OUT} = 0mA to 800mA, V_{IN} = 4.75V, 0°C ≤ T_J ≤ 125°C	TLV1117-33		1	15	
		I_{OUT} = 0mA to 800mA, V_{IN} = 6.5V, 0°C ≤ T_J ≤ 125°C	TLV1117-50		1	15	
	Load regulation (adjustable output)[6]	V_{IN} – V_{OUT} = 3V, 10mA ≤ I_{OUT} ≤ 800mA, T_J = 25°C	TLV1117		0.2		%
		V_{IN} – V_{OUT} = 3V, 10mA ≤ I_{OUT} ≤ 800mA, 0°C ≤ T_J ≤ 125°C				0.4	
		V_{IN} – V_{OUT} = 3V, 10mA ≤ I_{OUT} ≤ 800mA				0.5	
	Load regulation (new chip, fixed output)	1mA ≤ I_{OUT} ≤ 1A, V_{IN} ≥ 3.0V			0.1	0.75	%
						0.5	%/A
V_{DO}	Dropout voltage (legacy chip)[2]	I_{OUT} = 100mA, 0°C ≤ T_J ≤ 125°C			1.1	1.2	V
		I_{OUT} = 100mA			1.1	1.3	
		I_{OUT} = 500mA, 0°C ≤ T_J ≤ 125°C			1.15	1.25	
		I_{OUT} = 500mA			1.15	1.35	
		I_{OUT} = 800mA, 0°C ≤ T_J ≤ 125°C			1.2	1.3	
		I_{OUT} = 800mA			1.2	1.4	
	Dropout voltage (new chip, adjustable output) [2]	I_{OUT} = 100mA, T_J = 25°C			1.1		
		I_{OUT} = 100mA, –40°C ≤ T_J ≤ 125°C				1.3	
		I_{OUT} = 500mA, T_J = 25°C			1.15		
		I_{OUT} = 500mA, –40°C ≤ T_J ≤ 125°C				1.35	
		I_{OUT} = 800mA, T_J = 25°C			1.2		
		I_{OUT} = 800mA, –40°C ≤ T_J ≤ 125°C				1.4	
	Dropout voltage (new chip, fixed output) [9]	V_{IN} ≥ 3.0V, I_{OUT} = 1A			0.9	1.7	
I_{CL}	Output current limit (legacy chip)[3]	V_{IN} – V_{OUT} = 5V, T_J = 25°C	TLV1117x	0.8	1.2	1.6	A
	Output current limit (new chip, adjustable output)	V_{IN} – V_{OUT} = 5V, T_J = 25°C	TLV1117x-ADJ	0.8	1.2	1.6	
	Output current limit (new chip, fixed output)	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(nom)}$ + 1.5V or V_{IN} = 4.3V (whichever is greater)		1.1		1.6	
I_{SC}	Short-circuit current limit (new chip, fixed output)	V_{OUT} = 0V		150	250	350	mA
$I_{MIN(LOAD)}$ [7]	Minimum load current (legacy chip)	V_{IN} = 15V	TLV1117		1.7	5	mA
	Minimum load current (new chip, adjustable output)	V_{IN} = 15V, T_J = 25°C			1.7		
		V_{IN} = 15V				5	
	Minimum load current (new chip, fixed output)	V_{IN} = 16V				0	
I_Q	Quiescent current (legacy chip, fixed output)	V_{IN} ≤ 15V			5	10	mA
	Quiescent current (new chip, adjustable output)	V_{IN} ≤ 15V, T_J = 25°C			5		
		V_{IN} ≤ 15V				15	
	Quiescent current (new chip, fixed output)	I_{OUT} = 0mA			65	110	µA
	Thermal regulation (legacy chip)	T_A = 25°C, 30ms pulse			0.01	0.1	%/W
	Thermal regulation (new chip, adjustable output)	T_A = 25°C, 30ms pulse			0.01	0.1	
PSRR	Ripple rejection (legacy chip)	f_{RIPPLE} = 120Hz, V_{IN} – V_{OUT} = 3V, V_{RIPPLE} = $1V_{PP}$		60	75		dB
	Ripple rejection (new chip, adjustable output)	f_{RIPPLE} = 120Hz, V_{IN} – V_{OUT} = 3V, V_{RIPPLE} = $1V_{PP}$, T_J = 25°C			75		
		f_{RIPPLE} = 120Hz, V_{IN} – V_{OUT} = 3V, V_{RIPPLE} = $1V_{PP}$		60			
	Ripple rejection (new chip, fixed output)	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 300mA, f = 120Hz			70		

5.6 Electrical Characteristics (continued)

specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.5V or V_{IN} = 2.5V (whichever is greater), I_{OUT} = 10mA, C_{IN} = 1.0µF and C_{OUT} = 1.0µF (unless otherwise noted); typical values are at T_J= 25°C.

PARAMETER		TEST CONDITIONS(1)	MIN (4)	TYP (5)	MAX (4)	UNIT
I_{ADJ}	ADJ pin current (legacy chip)			80	120	µA
	ADJ pin current (new chip, adjustable output)	T_J = 25°C		60		
					120	
ΔI_{ADJ}	Adjust pin current change (legacy chip)	V_{IN} – V_{OUT} = 1.4V to 10V, I_{OUT}= 10mA to 800mA, 0°C ≤ T_J ≤ 125°C		0.2	5	µA
		V_{IN} – V_{OUT} = 1.4V to 10V, I_{OUT}= 10mA to 800mA		0.2	10	
	Adjust pin current change (new chip, adjustable output)	V_{IN} – V_{OUT} = 1.4V to 10V, I_{OUT}= 10mA to 800mA, T_J = 125°C		0.2		
		V_{IN} – V_{OUT} = 1.4V to 10V, I_{OUT}= 10mA to 800mA			10	
	Temperature stability	T_J = Full range		0.5		%
	Long-term stability	1000 hours, no load, T_A = 125°C		0.3		%
V_n	RMS output noise (legacy chip)	% of V_{OUT}, f = 10Hz to 100kHz		0.003		%
	RMS output noise (new chip, adjustable output)	% of V_{OUT}, f = 10Hz to 10kHz		0.003		
	RMS output noise (new chip, fixed output)	BW = 10Hz to 100kHz, V_{IN} = 3.3V, V_{OUT} = 0.8V, I_{OUT} = 100mA		60		$µV_{RMS}$
$I_{PULLDOWN}$	Output pulldown current (new chip, fixed output) (10)	V_{IN} = 1.8V, V_{OUT} = 2.5V	0.7		1.1	mA
V_{UVLO+}	UVLO threshold rising (new chip, fixed output)	V_{IN} rising		2.2	2.4	V
V_{UVLO-}	UVLO threshold falling (new chip, fixed output)	V_{IN} falling	1.9			V
$V_{UVLO(HYS)}$	UVLO hysteresis (new chip, fixed output)			130		mV
$T_{SD(shutdown)}$	Thermal shutdown temperature (new chip, fixed output)	Temperature increasing		180		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature (new chip, fixed output)	Temperature falling		160		°C

(1) For legacy chip only: all characteristics are measured with a 10µF capacitor across the input and a 10µF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(2) Dropout is defined as the V_{IN} to V_{OUT} differential at which V_{OUT} drops 100mV below the value of V_{OUT}, measured at V_{IN} = $V_{OUT(nom)}$ + 1.5V.
(3) Current limit test specified under recommended operating conditions.
(4) For new chip, adjustable output only: all limits are specified by testing or statistical analysis.
(5) For new chip, adjustable output only: typical values represent the most likely parametric normal.
(6) For new chip, adjustable output only: load and line regulation are measured at constant junction room temperature.
(7) The minimum output current required to maintain regulation.
(8) Line regulation is measured with V_{IN} = $V_{OUT(NOM)}$ + 1.5V or 2.5V (whichever is greater)
(9) V_{DO} is measured with V_{IN} = 95% x $V_{OUT(nom)}$ for fixed output devices. V_{DO} is not measured for fixed output devices when V_{OUT} < 2.5V.
(10) $I_{PULLDOWN}$ is measured with V_{IN} = 1.8V (lower than UVLO falling threshold, with LDO in disabled state) and 2.5V applied on V_{OUT} externally.

5.7 Typical Characteristics

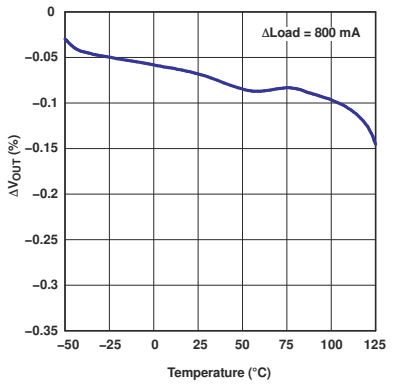
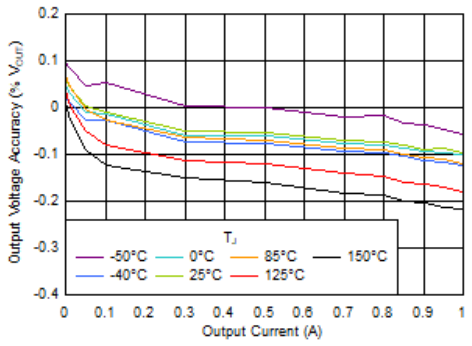
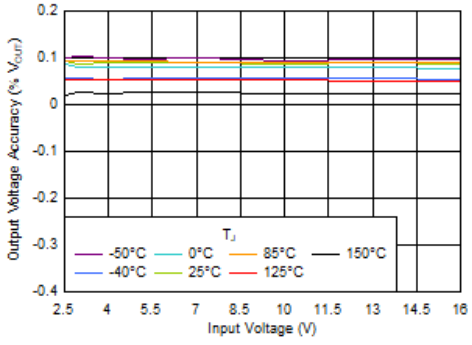


Figure 5-1. Load Regulation (Legacy Chip)



$V_{IN} \geq 3.0V$

Figure 5-2. V_{OUT} Accuracy vs I_{OUT} (Fixed Output, New Chip)



I_{OUT} = 10mA

Figure 5-3. V_{OUT} Accuracy vs V_{IN} (Fixed Output, New Chip)

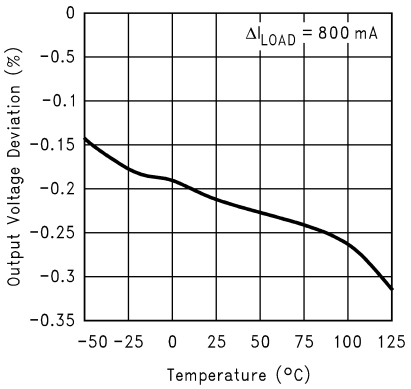


Figure 5-4. Load Regulation (Adjustable Output, New Chip)

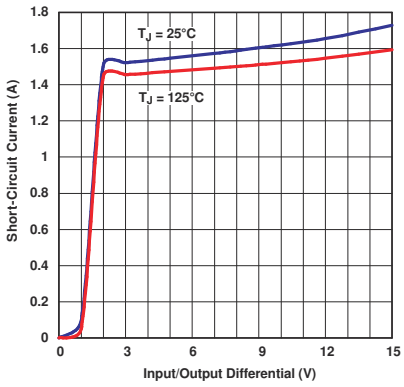
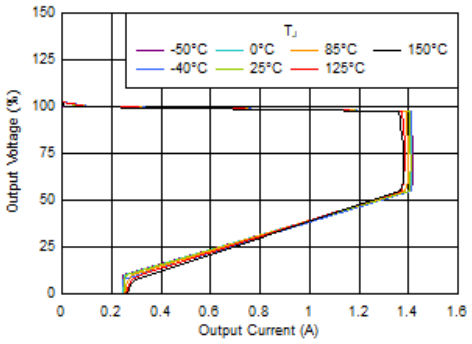


Figure 5-5. Short-Circuit Current vs (V_{IN} – V_{OUT}) (Legacy Chip)



$V_{IN} \geq 3.0V$

Figure 5-6. Foldback Current Limit vs Temperature (Fixed Output, New Chip)

5.7 Typical Characteristics (continued)

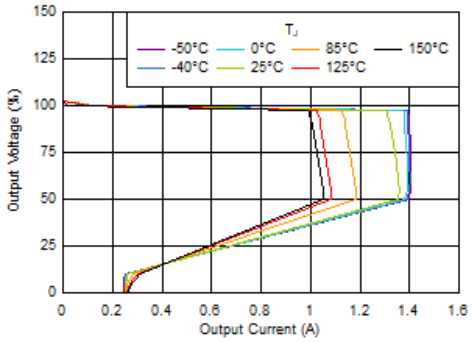


Figure 5-7. Foldback Current Limit vs Temperature (Fixed Output, New Chip)

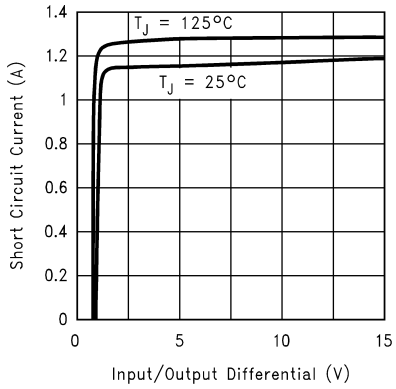


Figure 5-8. Short-Circuit Current (Adjustable Output, New Chip)

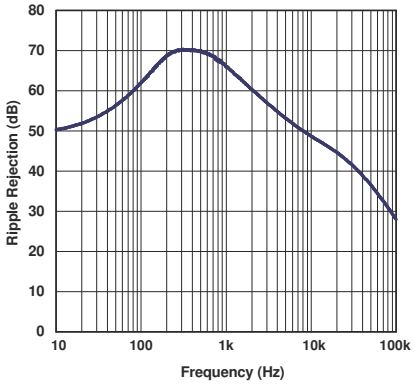


Figure 5-9. Ripple Rejection vs Frequency (Adjustable Output, Legacy Chip)

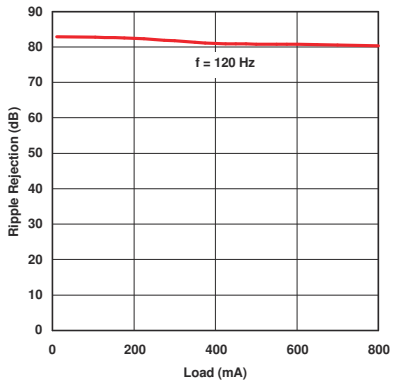
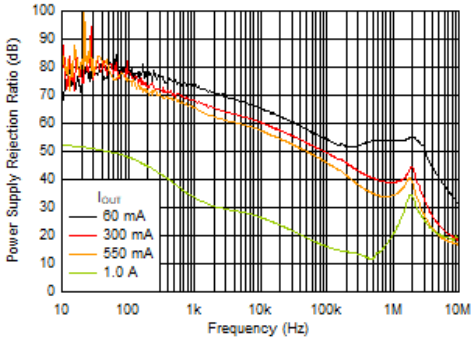
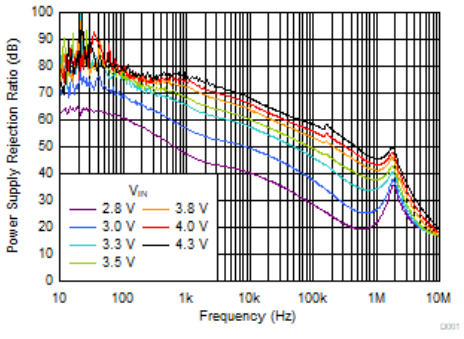


Figure 5-10. Ripple Rejection vs Load Current (Adjustable Output, Legacy Chip)



V_{OUT} = 1.8V, V_{IN} = 3.3V

Figure 5-11. Ripple Rejection vs Frequency (Fixed Output, New Chip)



V_{OUT} = 1.8V, I_{OUT} = 0.55A

Figure 5-12. Ripple Rejection vs Frequency (Fixed Output, New Chip)

5.7 Typical Characteristics (continued)

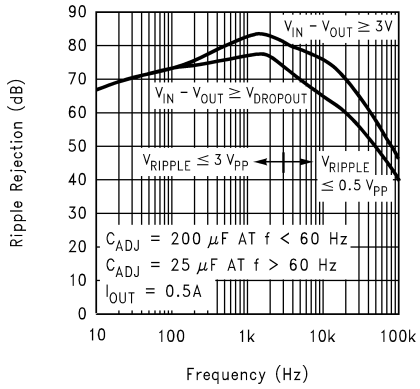


Figure 5-13. Ripple Rejection vs Frequency (Adjustable Output, New Chip)

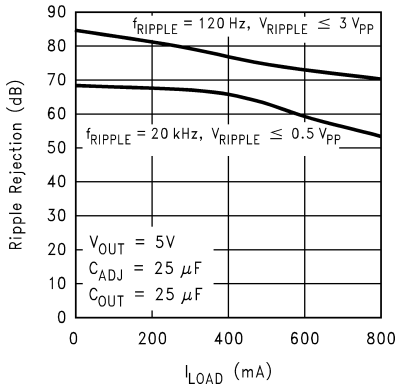


Figure 5-14. Ripple Rejection vs Frequency (Adjustable Output, New Chip)

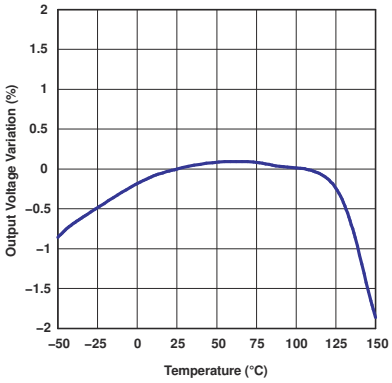


Figure 5-15. Temperature Stability (Legacy Chip)

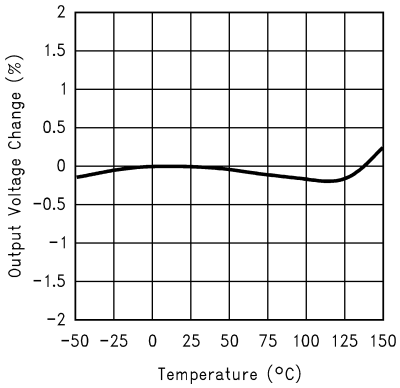


Figure 5-16. Temperature Stability (Adjustable Output, New Chip)

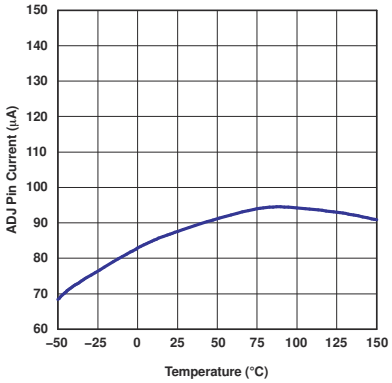


Figure 5-17. ADJ Pin Current vs Temperature (Legacy Chip)

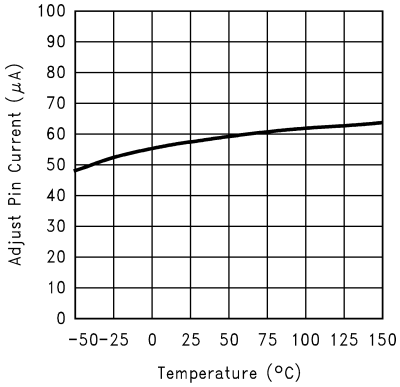


Figure 5-18. ADJ Pin Current vs Temperature (New Chip)

5.7 Typical Characteristics (continued)

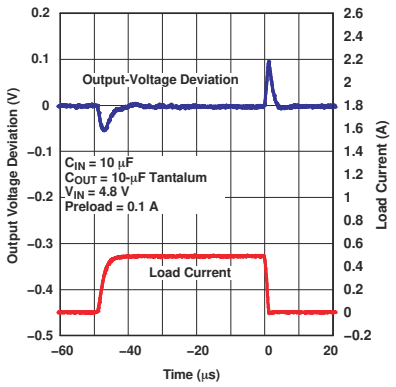
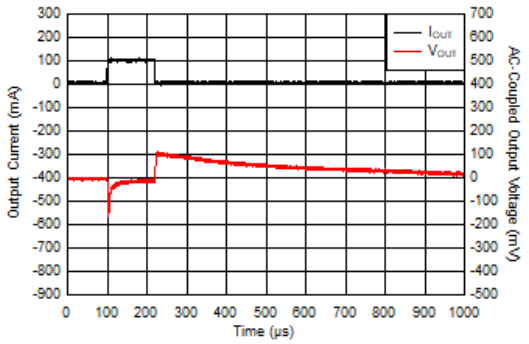
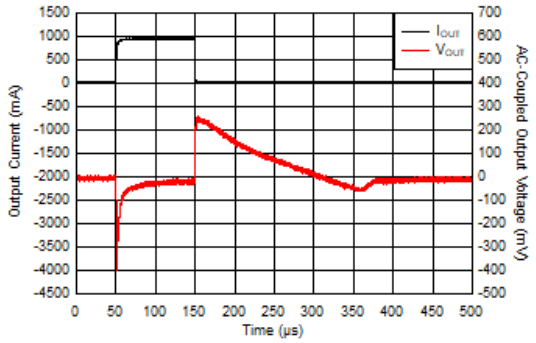


Figure 5-19. TLV1117-33 Load Transient Response (Legacy Chip)



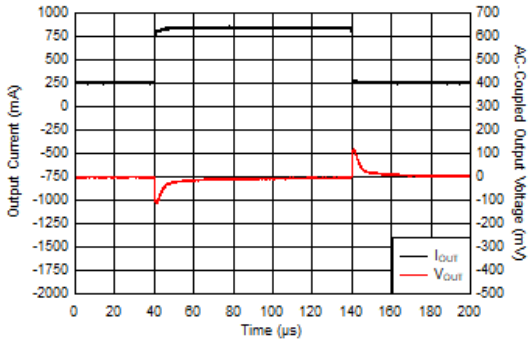
V_{IN} = 5V, V_{OUT} = 3.3V, ramp rate = 0.4A/µs

Figure 5-20. I_{OUT} Transient From 0mA to 100mA (Fixed Output, New Chip)



V_{IN} = 5V, V_{OUT} = 3.3V, ramp rate = 0.5A/µs

Figure 5-21. I_{OUT} Transient From 1mA to 1A (Fixed Output, New Chip)



V_{IN} = 5V, V_{OUT} = 3.3V, ramp rate = 0.8A/µs

Figure 5-22. I_{OUT} Transient From 250mA to 850mA (Fixed Output, New Chip)

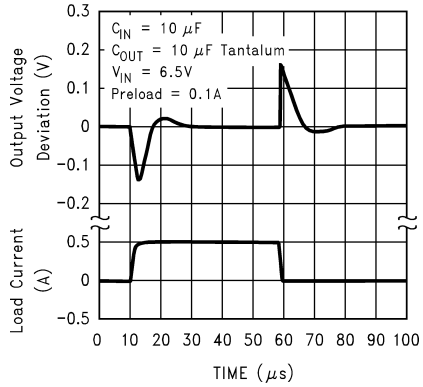


Figure 5-23. Load Transient Response (Adjustable Output, New Chip)

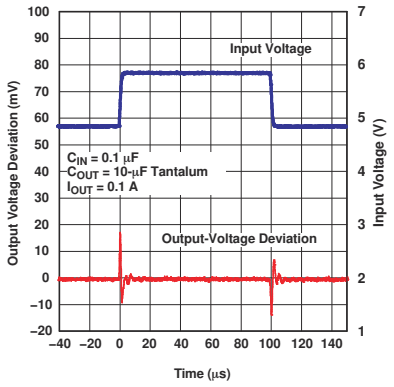
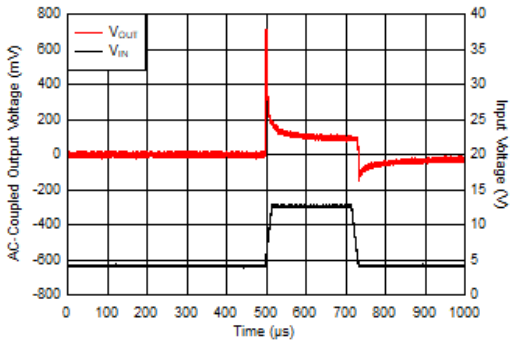


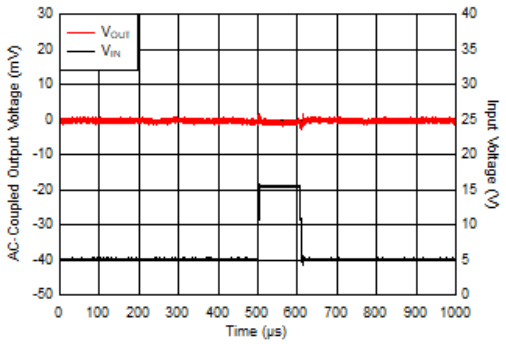
Figure 5-24. TLV1117-33 Line Transient Response (Legacy Chip)

5.7 Typical Characteristics (continued)



V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, V_{IN} ramp rate = 0.6V/µs

Figure 5-25. V_{IN} Transient in Dropout From 4V to 13V (Fixed Output, New Chip)



V_{OUT} = 3.3V, I_{OUT} = 33µA, V_{IN} ramp rate = 1.6V/µs

Figure 5-26. V_{IN} Transient From 5V to 16V (Fixed Output, New Chip)

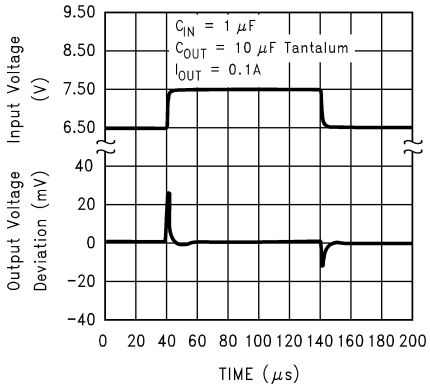


Figure 5-27. Line Transient Response (Adjustable Output, New Chip)

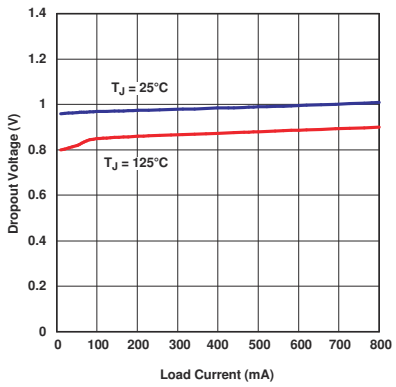
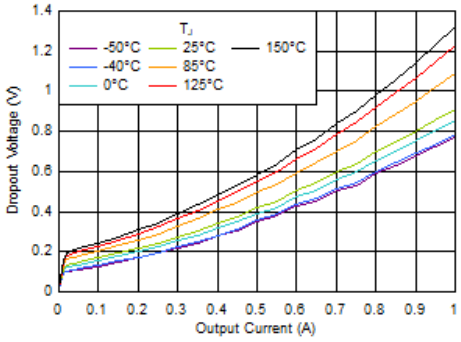
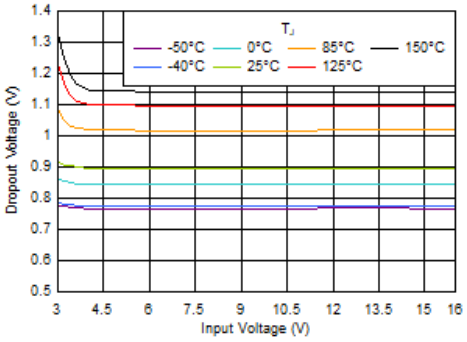


Figure 5-28. Dropout Voltage vs Load Current (Legacy Chip)



V_{IN} ≥ 3.0V

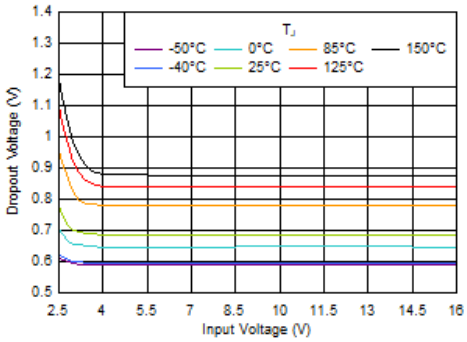
Figure 5-29. Dropout Voltage vs Load Current (Fixed Output, New Chip)



I_{OUT} = 1.0A

Figure 5-30. Dropout Voltage vs V_{IN} (Fixed Output, New Chip)

5.7 Typical Characteristics (continued)



I_{OUT} = 0.8A

Figure 5-31. Dropout Voltage vs V_{IN} (Fixed Output, New Chip)

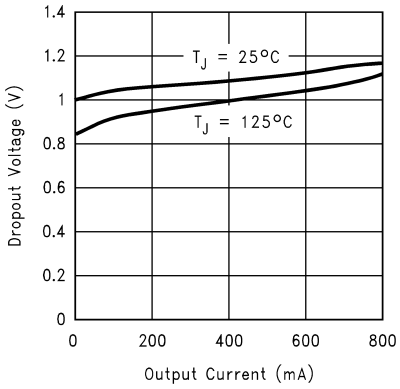
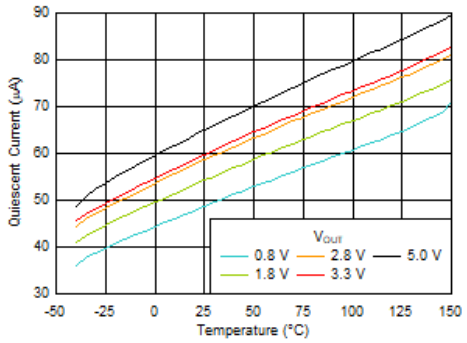
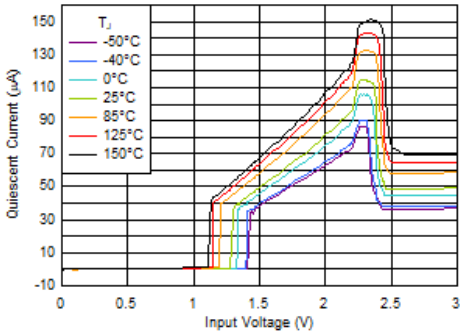


Figure 5-32. Dropout Voltage vs Load Current (Adjustable Output, New Chip)



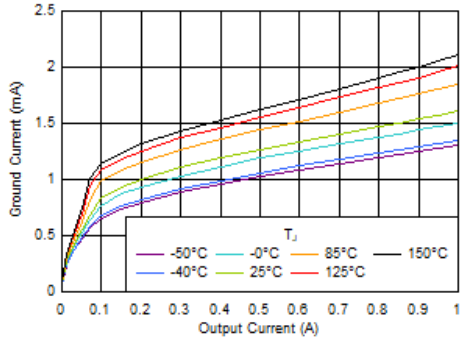
I_{OUT} = 0mA

Figure 5-33. I_Q vs Temperature (Fixed Output, New Chip)



I_{OUT} = 0mA

Figure 5-34. I_Q Increase Below Minimum V_{IN} (Fixed Output, New Chip)



$V_{IN} \geq 3.0V$

Figure 5-35. I_{GND} vs I_{OUT} (Fixed Output, New Chip)

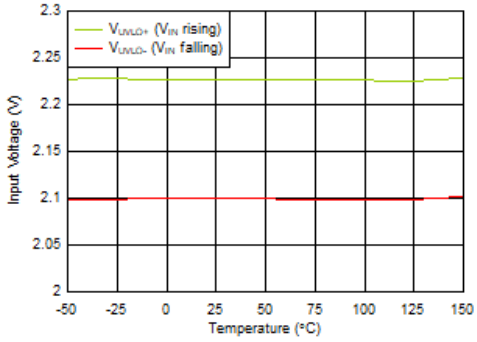
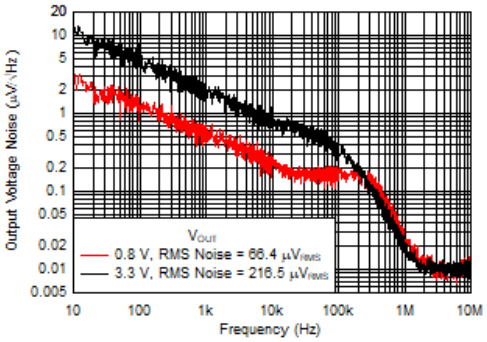


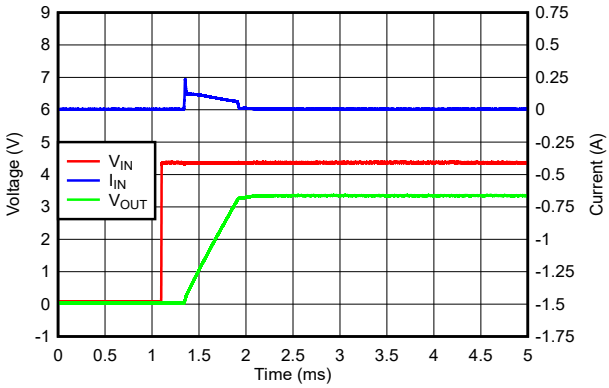
Figure 5-36. UVLO Thresholds vs Temperature (Fixed Output, New Chip)

5.7 Typical Characteristics (continued)



I_{OUT} = 0.1A, RMS noise BW = 10Hz to 100kHz

Figure 5-37. Output Noise (V_n) vs V_{OUT} (Fixed Output, New Chip)



I_{OUT} = 0.1A, C_{OUT} = 22μF

Figure 5-38. Inrush Current With 22μF at C_{OUT} (Fixed Output, New Chip)

6 Detailed Description

6.1 Overview

The TLV1117 is a positive low-dropout voltage regulator designed to provide up to 800mA of output current. The device is available in both fixed (1.5V to 5V), and adjustable (1.25V to 13.8V) output voltage configurations. For new chip configurations, all internal circuitry is designed to operate down to a 1.5V, input-to-output differential. Dropout voltage is specified at a maximum of 1.3V at 800mA, decreasing at lower load currents.

The fixed version (new chip) features integrated foldback current limit, thermal shutdown, internal output pulldown, and undervoltage lockout (UVLO). The adjustable version (new chip) develops a 1.25V reference voltage (V_{REF}) between the OUTPUT and the ADJ pin.

6.2 Functional Block Diagrams

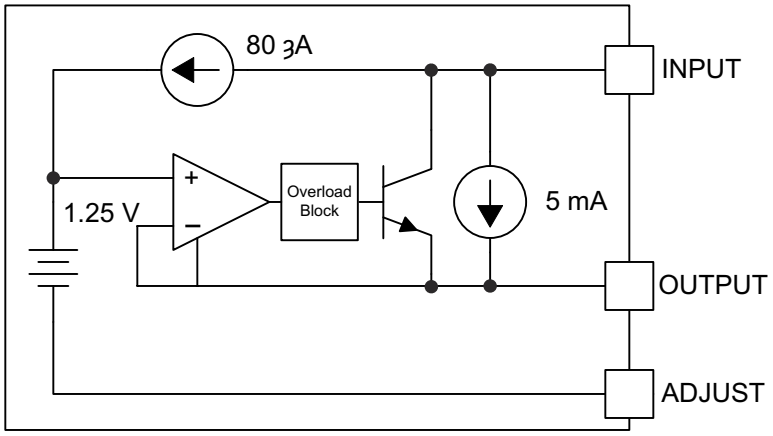


Figure 6-1. Functional Block Diagram (Legacy Chip)

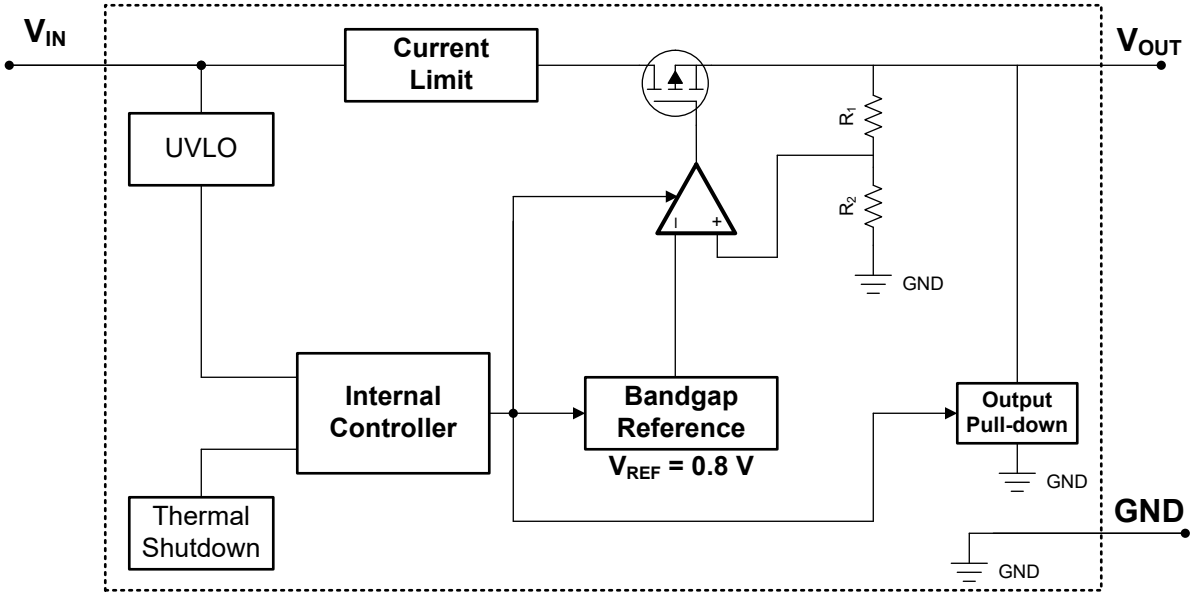


Figure 6-2. Functional Block Diagram (Fixed Output, New Chip)

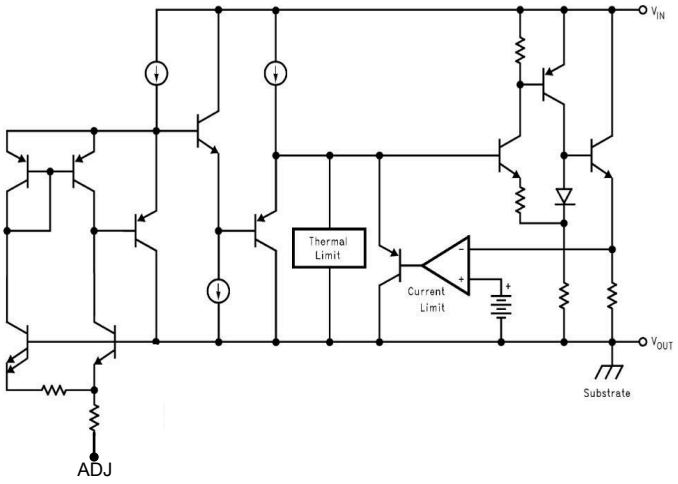


Figure 6-3. Functional Block Diagram (Adjustable Output, New Chip)

6.3 Feature Description

6.3.1 Dropout Voltage (Fixed Output, New Chip)

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.2 Foldback Current Limit (Fixed Output, New Chip)

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current termed the *short-circuit current limit (I_{SC})*. I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 50% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-4 shows a diagram of the foldback current limit.

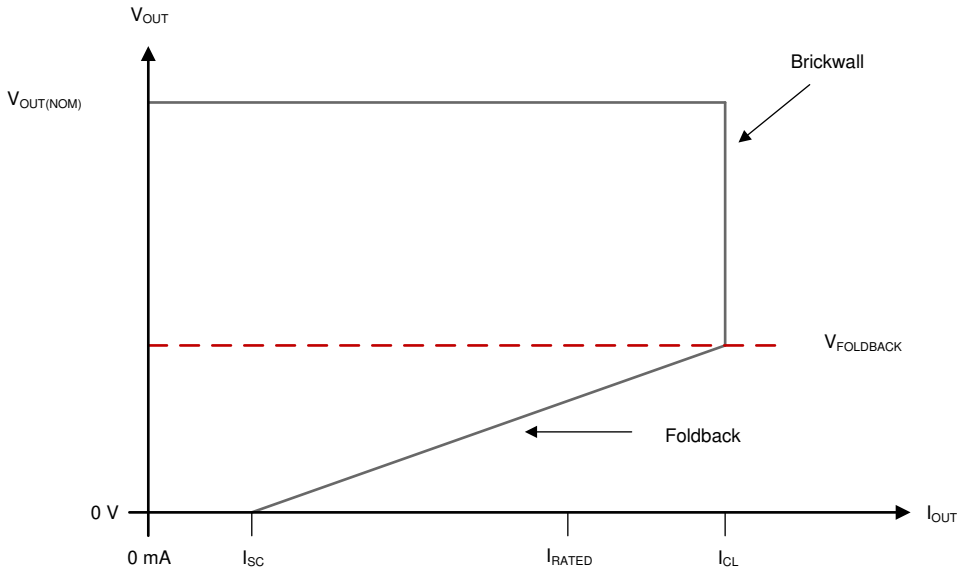


Figure 6-4. Foldback Current Limit

6.3.3 Undervoltage Lockout (Fixed Output, New Chip)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage. This circuit allows for a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.4 Thermal Shutdown (Fixed Output, New Chip)

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

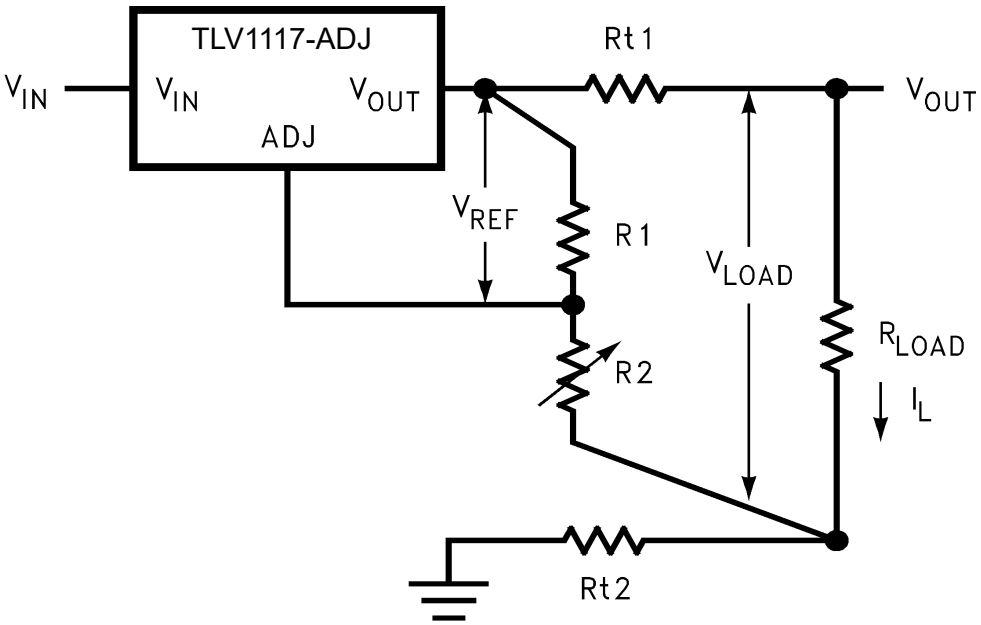
The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.5 Load Regulation (Adjustable Output, New Chip)

The TLV1117 regulates the voltage that appears between the output and adjust pins. In some cases, line resistances introduce errors to the voltage across the load. To obtain the best load regulation, a few precautions are needed.

Figure 6-5 shows a diagram using the adjustable regulator. Best performance is obtained with the positive side of resistor R1 tied directly to the regulator output terminal rather than near the load. This layout eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 5V regulator with 0.05Ω resistance between the regulator and load has load regulation resulting from the line resistance of 0.05Ω × I_L. If R1 (equal to 125Ω) is connected near the load, the effective line resistance is 0.05Ω × (1 + R2 / R1). In this case, the effective line resistance is four times worse. In addition, the ground side of the resistor R2 is returned near the ground of the load to provide remote ground sensing and improve load regulation.



$$V_{LOAD} = V_{REF} (R1 + R2)/R1 - I_L Rt1$$

Figure 6-5. Best Load Regulation Using Adjustable Output Regulator

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison (Fixed Output, New Chip)

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$

6.4.2 Normal Operation (Fixed Output)

The device regulates to the nominal output voltage when the following conditions are met:

For the new chip:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

For the legacy chip:

- The device passes the bias current to the OUT pin. The load or feedback consumes the minimum load current captured in the *Electrical Characteristics* for regulation or the output is potentially too high.

6.4.3 Dropout Operation (Fixed Output, New Chip)

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the regulator exits dropout, the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$. During this time, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During dropout exit, the device pulls the pass transistor back from being driven fully on.

6.4.4 Protection Diodes (Adjustable Output, New Chip)

Under normal operation, the TLV1117 regulators do not need protection diodes. With the adjustable device, the internal resistance between the ADJ and output terminals limits the current. No diode is needed to divert the current around the regulator even with the capacitor on the ADJ terminal. The ADJ pin withstands a transient signal of ±25V with respect to the output voltage without damaging the device.

When an output capacitor is connected to a regulator and the input is shorted to ground, the output capacitor discharges into the regulator output. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and rate of decrease of V_{IN}. In the TLV1117 regulators, the internal diode between the output and input pins withstands microsecond surge currents of 10A to 20A. With an extremely large output capacitor (≥1000µF), and with the input instantaneously shorted to ground, the regulator is potentially damaged.

In this case, as shown in Figure 6-6, place an external diode between the output and input pins to protect the regulator.

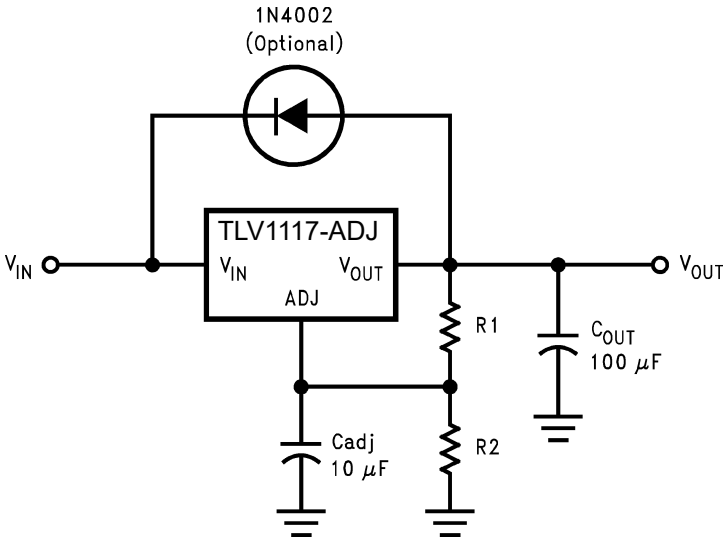


Figure 6-6. Regulator With Protection Diode

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV1117 is a versatile and high-performance, linear regulator with a wide temperature range and tight line and load regulation operation. An output capacitor is required to further improve transient response and stability. For the adjustable option, the ADJ pin can also be bypassed to achieve very-high, ripple-rejection ratios. The TLV1117 is versatile in the device applications, including being used as a post regulator for DC/DC converters, battery chargers, and microprocessor supplies.

7.1.1 Recommended Capacitor Types (Fixed Output, New Chip)

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements (Fixed Output, New Chip)

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time, load, or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.1.3 Reverse Current (Fixed Output, New Chip)

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which potentially exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 7-1 shows one approach for protecting the device.

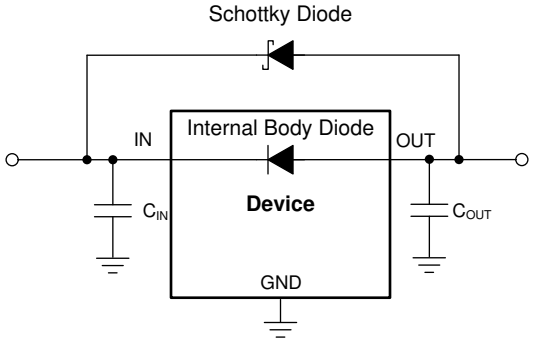


Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.4 Power Dissipation (Fixed Output, New Chip)

Circuit reliability requires proper consideration pf the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Note

Power dissipation is minimized, and therefore greater efficiency achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. The following equation describes this relationship.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. This resistance therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance.

7.1.5 Estimating Junction Temperature (Fixed Output, New Chip)

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the linear regulator junction temperatures when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the printed circuit board (PCB) surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (4)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (5)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use the metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2 Typical Application (Adjustable Output)

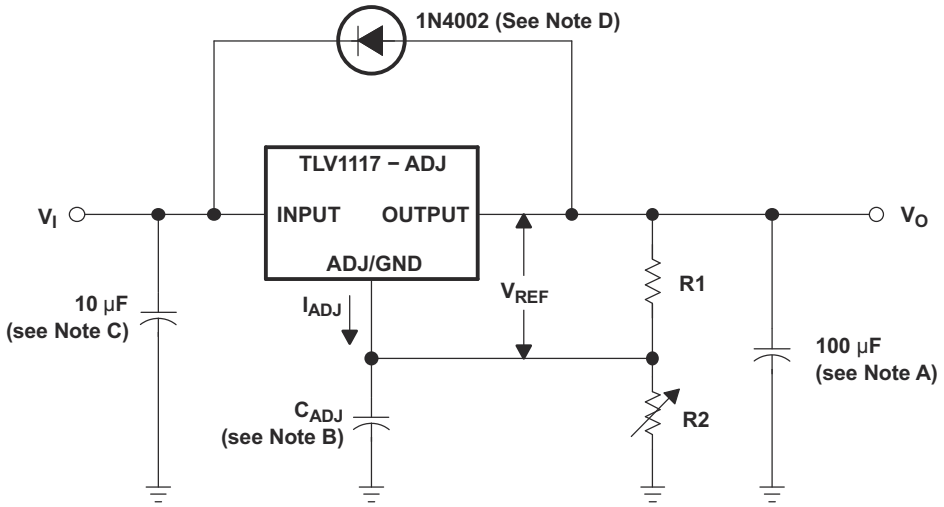


Figure 7-2. Basic Adjustable Regulator

Note

The *Design Requirements (Adjustable Output)* section lists details for notes referenced in Figure 7-2.

The adjustable version of the TLV1117 takes a 2.7V to 15V input. The V_{REF} voltage refers to the voltage between the output and the ADJUST pin, typically 1.25V. The V_{REF} voltage causes current to flow across R1, which is the same current that flows across R2 (minus the negligible 50µA I_{ADJ}). Therefore, adjust R2 to create a larger

voltage drop from GND and set the output voltage. The output voltage equation is described in the *Detailed Design Procedure (Adjustable Output)* section.

7.2.1 Design Requirements (Adjustable Output)

The bullets in this section are in reference to Figure 7-2.

- Note A: Output capacitor selection is critical for regulator stability. Larger C_{OUT} values benefit the regulator by improving transient response and loop stability. This device is designed to be stable with tantalum and aluminum electrolytic output capacitors with an ESR between 0.2Ω and 10Ω.
- Note B: Use C_{ADJ} to improve ripple rejection. If C_{ADJ} is used, a make sure to use a C_{OUT} that is larger in value than C_{ADJ}.
- Note C: Use C_{IN} if the TLV1117 is not located near the power-supply filter.
- Note D: Use an external diode to protect the regulator if the input is instantaneously shorted to GND.

7.2.2 Detailed Design Procedure

7.2.2.1 Detailed Design Procedure (Fixed Output, New Chip)

For this design example, the 3.3V, fixed-version TLV1117-3.3 is selected and is powered by a standard 12V input supply. Keep the dropout voltage (V_{DO}) within the TLV1117-3.3 dropout voltage specification for the 3.3V output voltage option. This voltage level keeps the device in regulation under all load and temperature conditions for this design. Use a 1.0µF output capacitor for excellent load transient response. The input capacitor is optional and is used to reduce the input impedance of the circuit and improve the transient response.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude.

7.2.2.2 Detailed Design Procedure (Adjustable Output)

Calculate the output voltage with the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right) + \left(I_{ADJ} \times R_2\right) \quad (6)$$

Neglecting I_{ADJ} is permissible in most applications because the value is approximately 50µA (new chip) and 80µA (legacy chip).

7.2.3 Application Curves

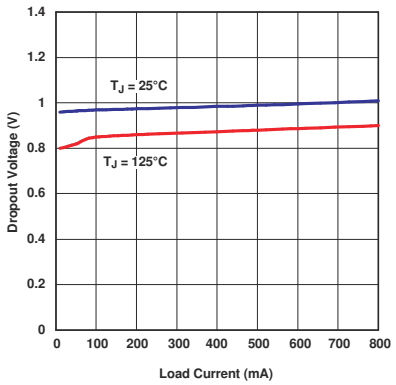


Figure 7-3. Dropout Voltage vs Load Current (Legacy Chip)

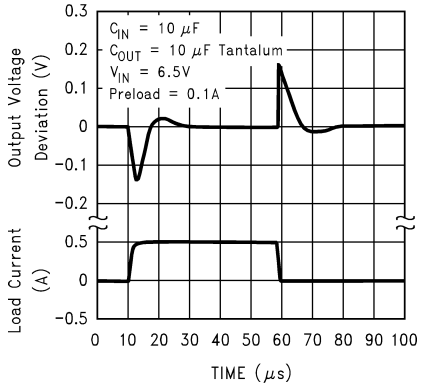


Figure 7-4. Load Transient Response (Adjustable Output, New Chip)

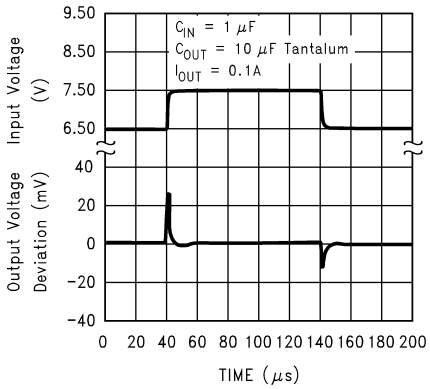
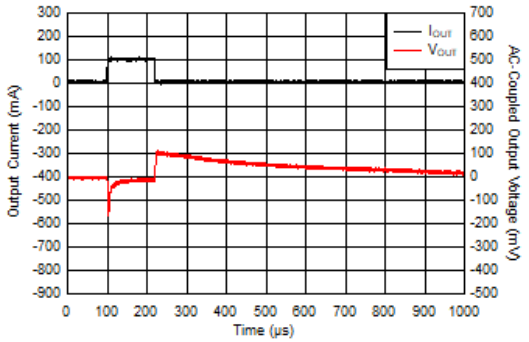
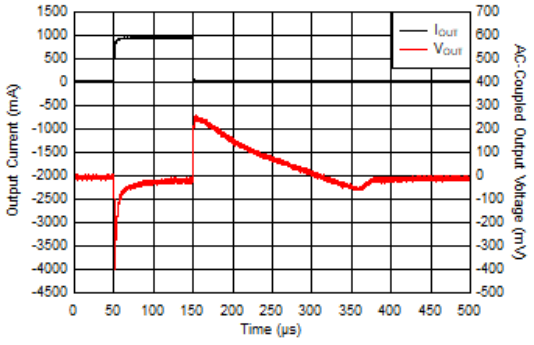


Figure 7-5. Line Transient Response (Adjustable Output, New Chip)



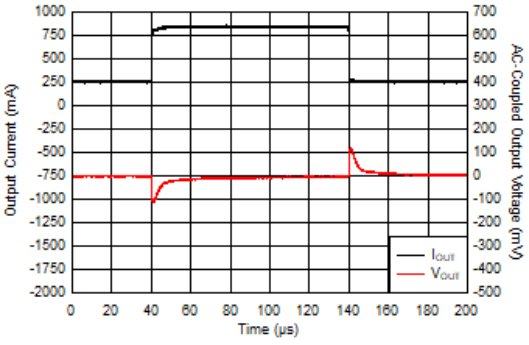
V_{IN} = 5V, V_{OUT} = 3.3V, ramp rate = 0.4A/µs

Figure 7-6. Load Transient Response, 1mA to 100mA (Fixed Output, New Chip)



V_{IN} = 5V, V_{OUT} = 3.3V, ramp rate = 0.5A/µs

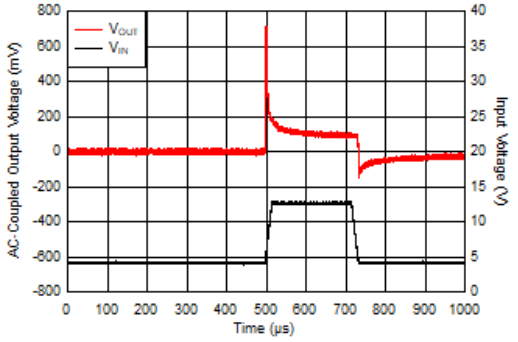
Figure 7-7. Load Transient Response, 1mA to 1A (Fixed Output, New Chip)



V_{IN} = 5V, V_{OUT} = 3.3V, ramp rate = 0.8A/µs

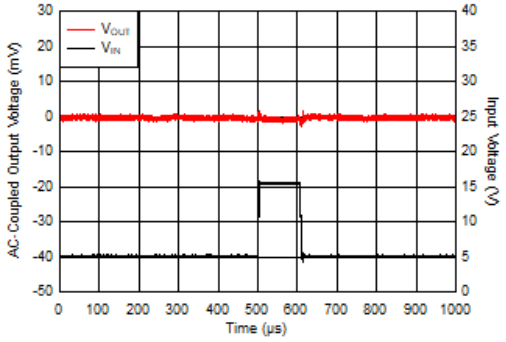
Figure 7-8. Load Transient Response, 250mA to 850mA (Fixed Output, New Chip)

7.2.3 Application Curves (continued)



V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, V_{IN} ramp rate = 0.6V/µs

Figure 7-9. Line Transient Response, 4V to 13V (Fixed Output, New Chip)



V_{OUT} = 3.3V, I_{OUT} = 33µA, V_{IN} ramp rate = 1.6V/µs

Figure 7-10. Line Transient Response, 5V to 16V (Fixed Output, New Chip)

7.3 Power Supply Recommendations

The fixed and adjustable versions of the TLV1117 have different recommended ranges of operating voltage. See the *Recommended Operating Conditions* table for specific operating ranges.

7.4 Layout

7.4.1 Layout Guidelines

One or two input capacitors are recommended if the TLV1117 is not located near the power-supply output filter capacitor. These capacitors filter high-frequency noise and mitigate brief voltage surges from the input. Make sure traces on the device input and output pins are wide enough to support the full current range needed in the application to minimize I×R drop.

7.4.2 Layout Example

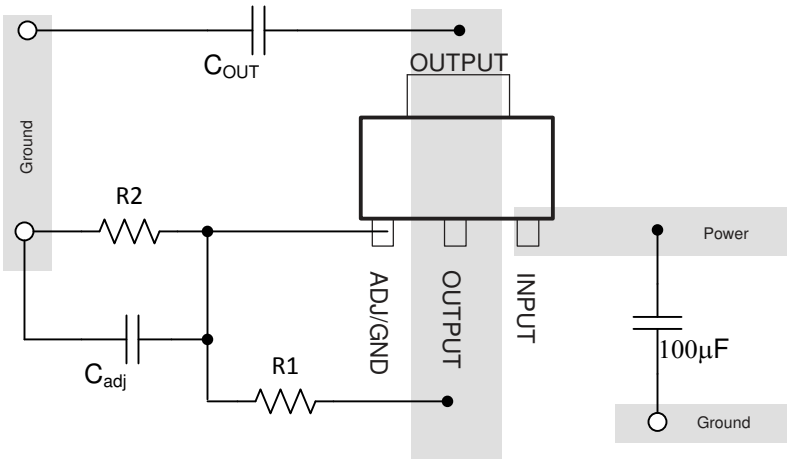


Figure 7-11. Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1) (2)	V_{OUT}
TLV1117-**aaxyyyz** Legacy chip	**aa** is the nominal output voltage (for example 33 = 3.3V). **x** is the operating temperature range. **yyy** is the package designator. **z** is the package quantity.Fab source on the packaging label, CSO: SFB.
TLV1117-**aaxyyyz** New chip	**aa** is the nominal output voltage (for example 33 = 3.3V). **x** is the operating temperature range. **yyy** is the package designator. **z** is the package quantity.Fab source on the packaging label, CSO: RFB or CSO: FFAB.

(1) Because this device ships with either legacy or new silicon, the product is identified with the fab source on the packaging label. (CSO: RFB, CSO: FFAB = new chip; CSO: SFB = legacy chip). Performance associated with the new and legacy chip is distinguished as such throughout the document.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (January 2023) to Revision N (April 2025)	Page
• Added new chip devices to document	1
• Changed entire document to identify the features and differences of the legacy chip and new chip and the adjustable and fixed versions of the device	1
• Deleted *Disabled* row from *Device Functional Mode Comparison* table	21
• Added *Device Nomenclature* section	29

Changes from Revision L (October 2014) to Revision M (January 2023)	Page
• Added drop-in replacement bullet to *Features* section	1
• Added *Application Information* section	23

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1117-15CDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T2
TLV1117-15CDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T2
TLV1117-15CDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T2
TLV1117-15CDRJR	Active	Production	SON (DRJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYH
TLV1117-15IDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T3
TLV1117-15IDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T3
TLV1117-15IKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	ZF15
TLV1117-18CDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T4
TLV1117-18CDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T4
TLV1117-18CDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T4
TLV1117-18CDRJR	Active	Production	SON (DRJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYK
TLV1117-18CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	ZE18
TLV1117-18IDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T5
TLV1117-18IDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T5
TLV1117-18IDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T5
TLV1117-18IDRJR	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYL
TLV1117-18IKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	ZF18
TLV1117-25CDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T6
TLV1117-25CDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T6
TLV1117-25CDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	T6
TLV1117-25CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	ZE25
TLV1117-25IDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T8
TLV1117-25IDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T8
TLV1117-25IDRJR	Active	Production	SON (DRJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYN
TLV1117-33CDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	V3
TLV1117-33CDCYG3	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	V3
TLV1117-33CDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	V3
TLV1117-33CDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	V3
TLV1117-33CDRJR	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYP

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1117-33CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	ZE33
TLV1117-33IDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	(V3, VS)
TLV1117-33IDCYG3	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	(V3, VS)
TLV1117-33IDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VS
TLV1117-33IDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VS
TLV1117-33IDRJR	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYR
TLV1117-33IKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	ZF33
TLV1117-50CDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	VT
TLV1117-50CDCYG3	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	VT
TLV1117-50CDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	VT
TLV1117-50CDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	VT
TLV1117-50CDRJR	Active	Production	SON (DRJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZE50
TLV1117-50CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	ZE50
TLV1117-50IDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VU
TLV1117-50IDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VU
TLV1117-50IDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	VU
TLV1117-50IDRJR	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZF50
TLV1117-50IDRJRG4	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZF50
TLV1117-50IKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	ZF50
TLV1117CDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	V4
TLV1117CDCYG3	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	V4
TLV1117CDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	V4
TLV1117CDCYR.Z	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	V4
TLV1117CDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	V4
TLV1117CDRJR	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYS
TLV1117CKCS	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TLV1117C
TLV1117CKTTR	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	TLV1117C
TLV1117CKTTRG3	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	TLV1117C
TLV1117CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	TV1117

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1117CKVURG3.Z	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TV1117
TLV1117IDCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	V2
TLV1117IDCYG3	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	V2
TLV1117IDCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	V2
TLV1117IDCYR.Z	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	V2
TLV1117IDCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	V2
TLV1117IDRJR	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYT
TLV1117IKCS	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	TLV1117I
TLV1117IKCSE3	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	TLV1117I
TLV1117IKTTR	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TLV1117I
TLV1117IKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TY1117
TLV1117IKVURG3.Z	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TY1117

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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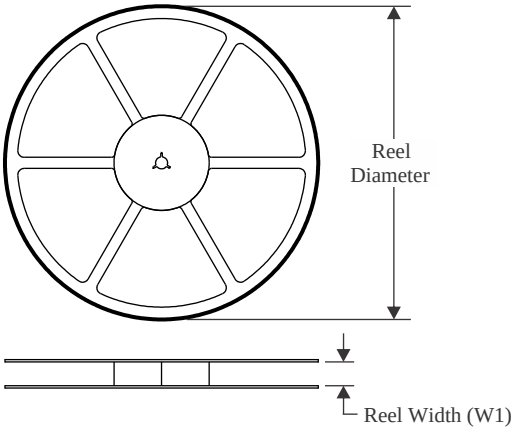
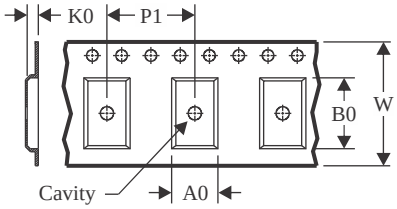
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

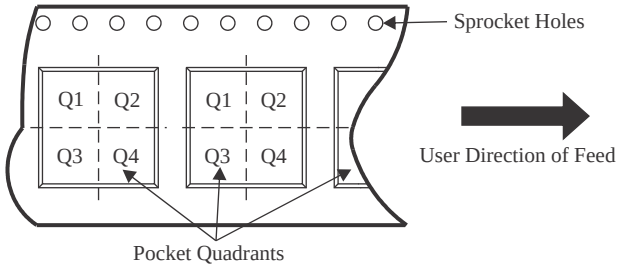


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

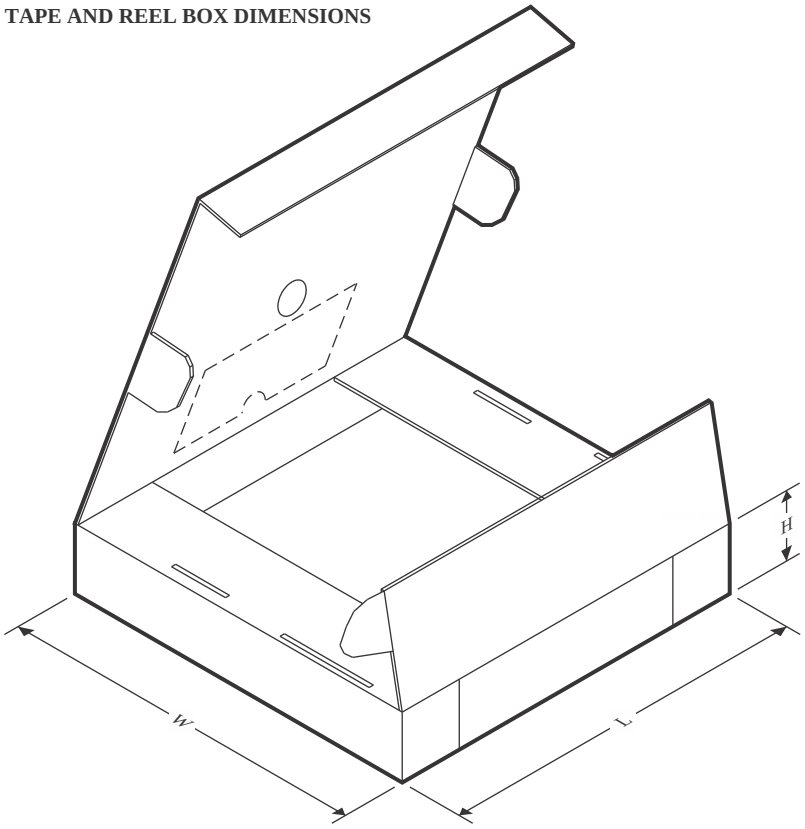


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117-15CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-15CDRJR	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-15IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-15IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-15IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-18CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-18CDRJR	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-18CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-18IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-18IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-18IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-25CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-25CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-25CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-25IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-25IDRJR	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117-33CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-33CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-33CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-33CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-33IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-33IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-33IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-33IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-50CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-50CDRJR	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-50CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-50IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-50IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-50IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-50IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TLV1117CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117IKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TLV1117IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

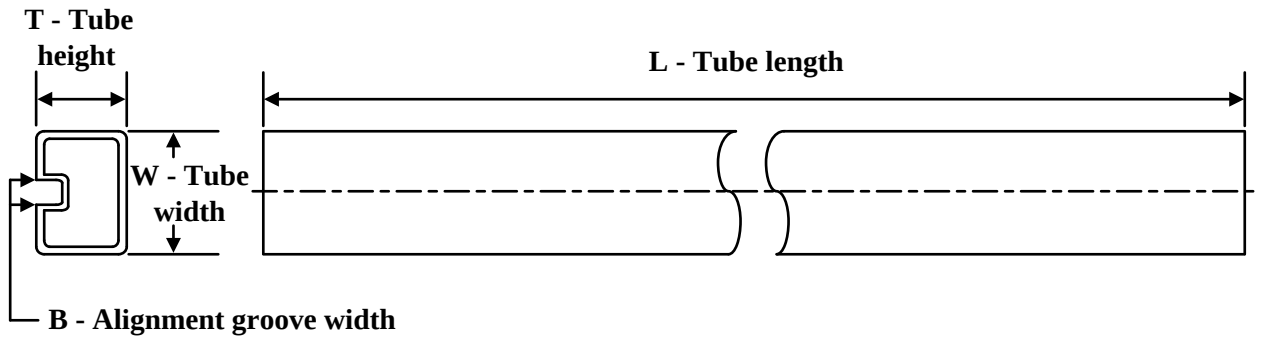


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117-15CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-15CDRJR	SON	DRJ	8	3000	367.0	367.0	35.0
TLV1117-15IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-15IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-15IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-18CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-18CDRJR	SON	DRJ	8	3000	367.0	367.0	35.0
TLV1117-18CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-18IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-18IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-18IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-25CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-25CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-25CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-25IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-25IDRJR	SON	DRJ	8	3000	367.0	367.0	35.0
TLV1117-33CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-33CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117-33CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-33CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-33IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-33IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-33IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-33IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-50CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-50CDRJR	SON	DRJ	8	3000	367.0	367.0	35.0
TLV1117-50CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-50IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-50IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-50IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-50IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TLV1117CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117IKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TLV1117IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0

TUBE



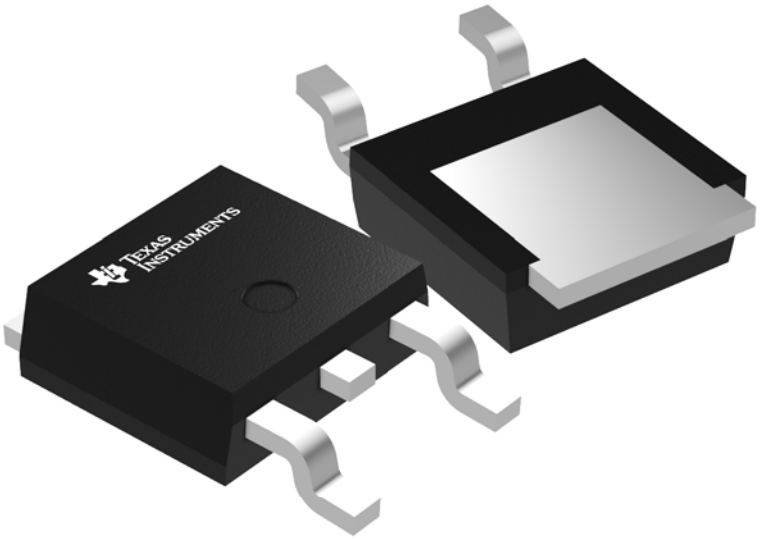
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV1117-15CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-15IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-18CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-18IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-25CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-25IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-33CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-33CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-33IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-33IDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-50CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-50CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-50IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117CDCY	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
TLV1117CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117CDCYG3	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
TLV1117CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117IDCY	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
TLV1117IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117IDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117IDCYG3	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
TLV1117IKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117IKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117IKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117IKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



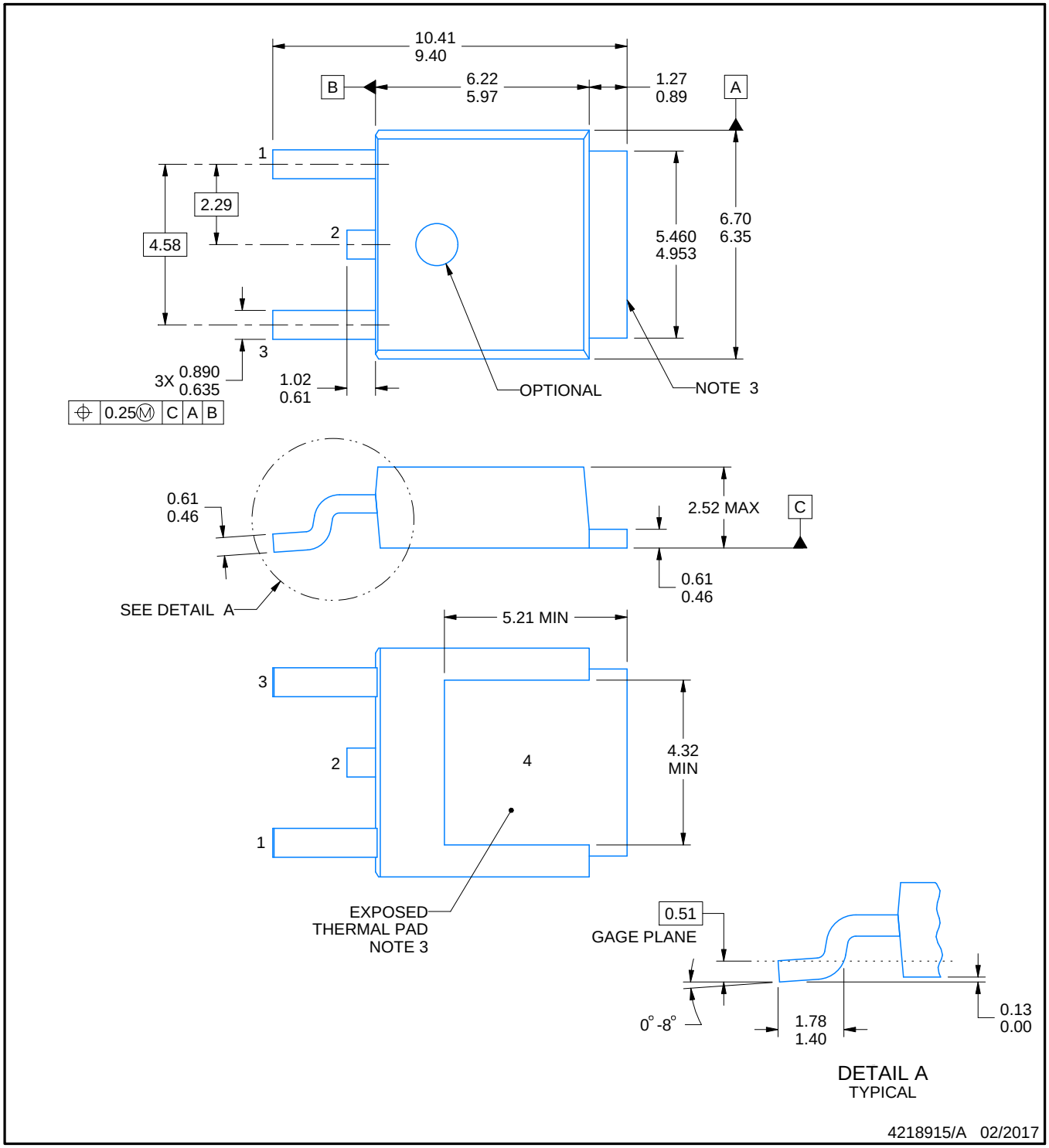
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

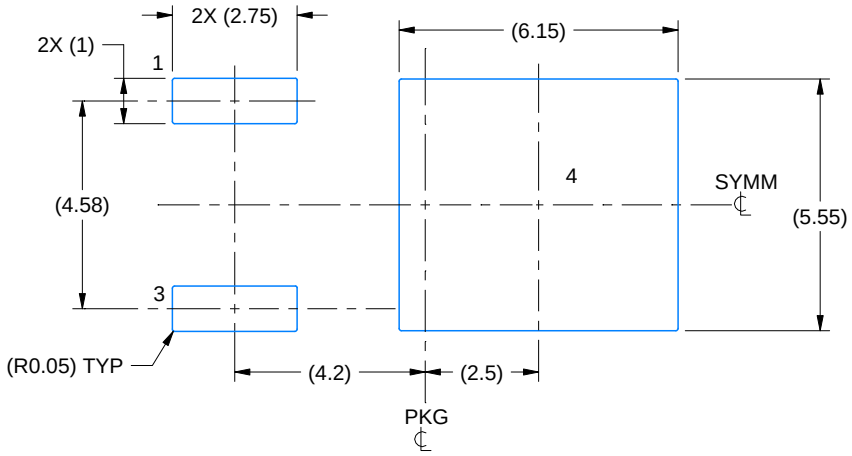
TO-252 - 2.52 mm max height

TO-252

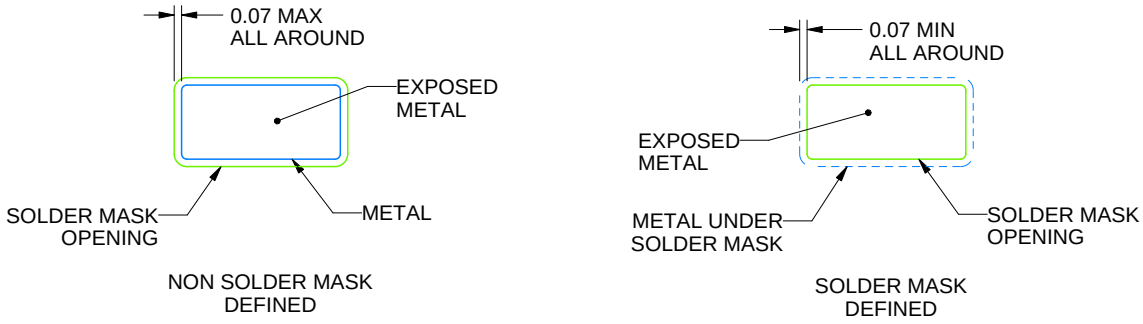


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

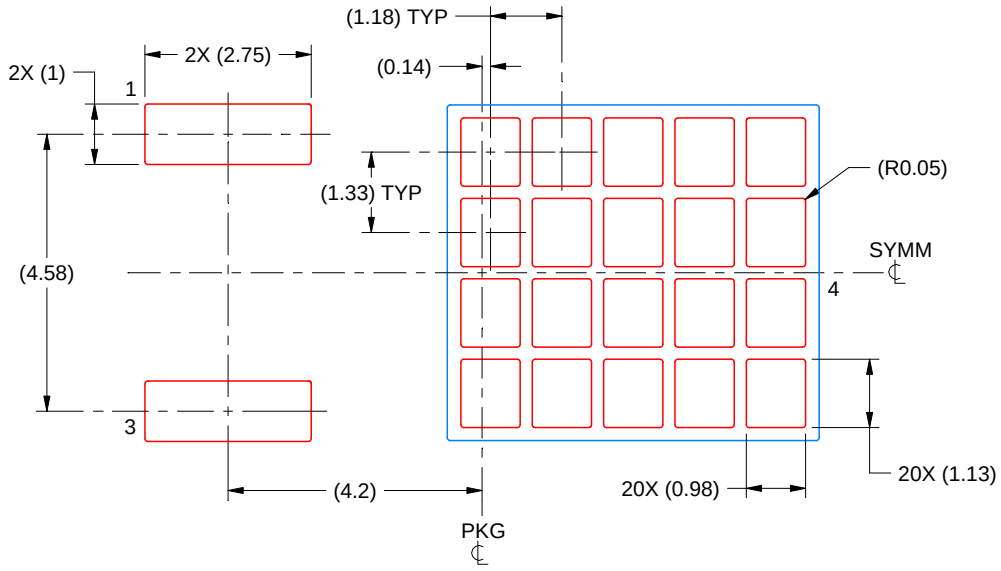
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

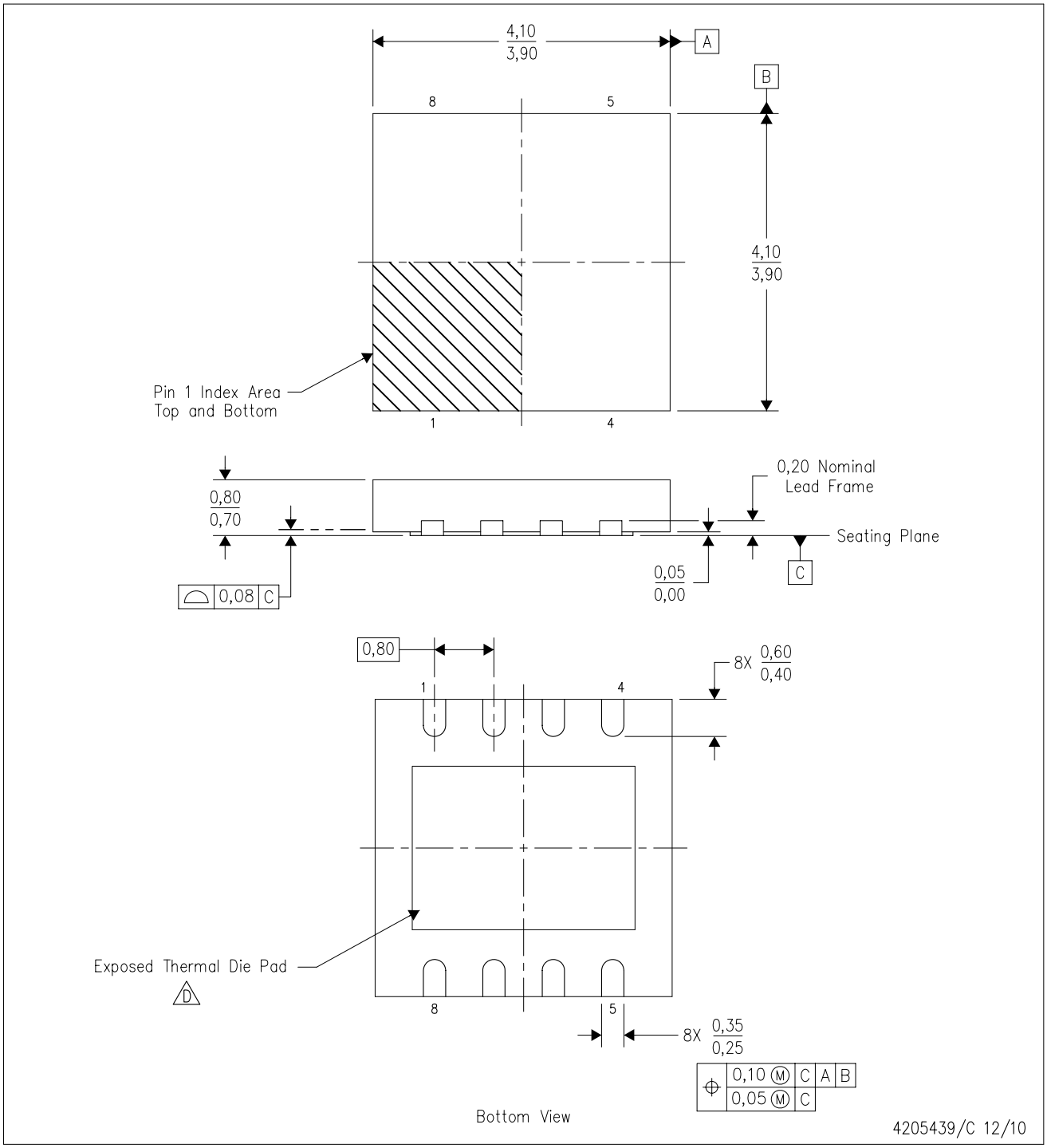
EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

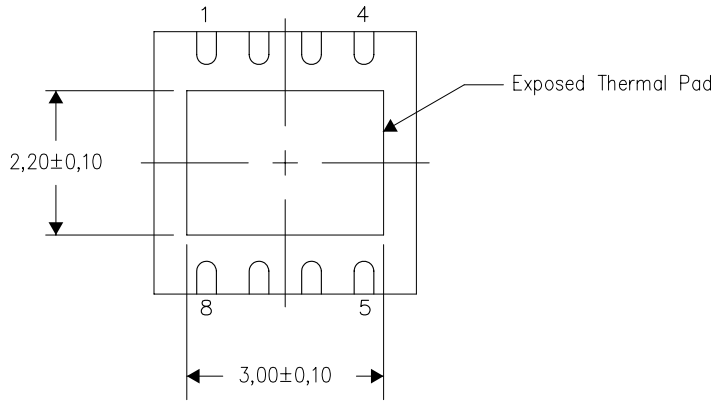
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



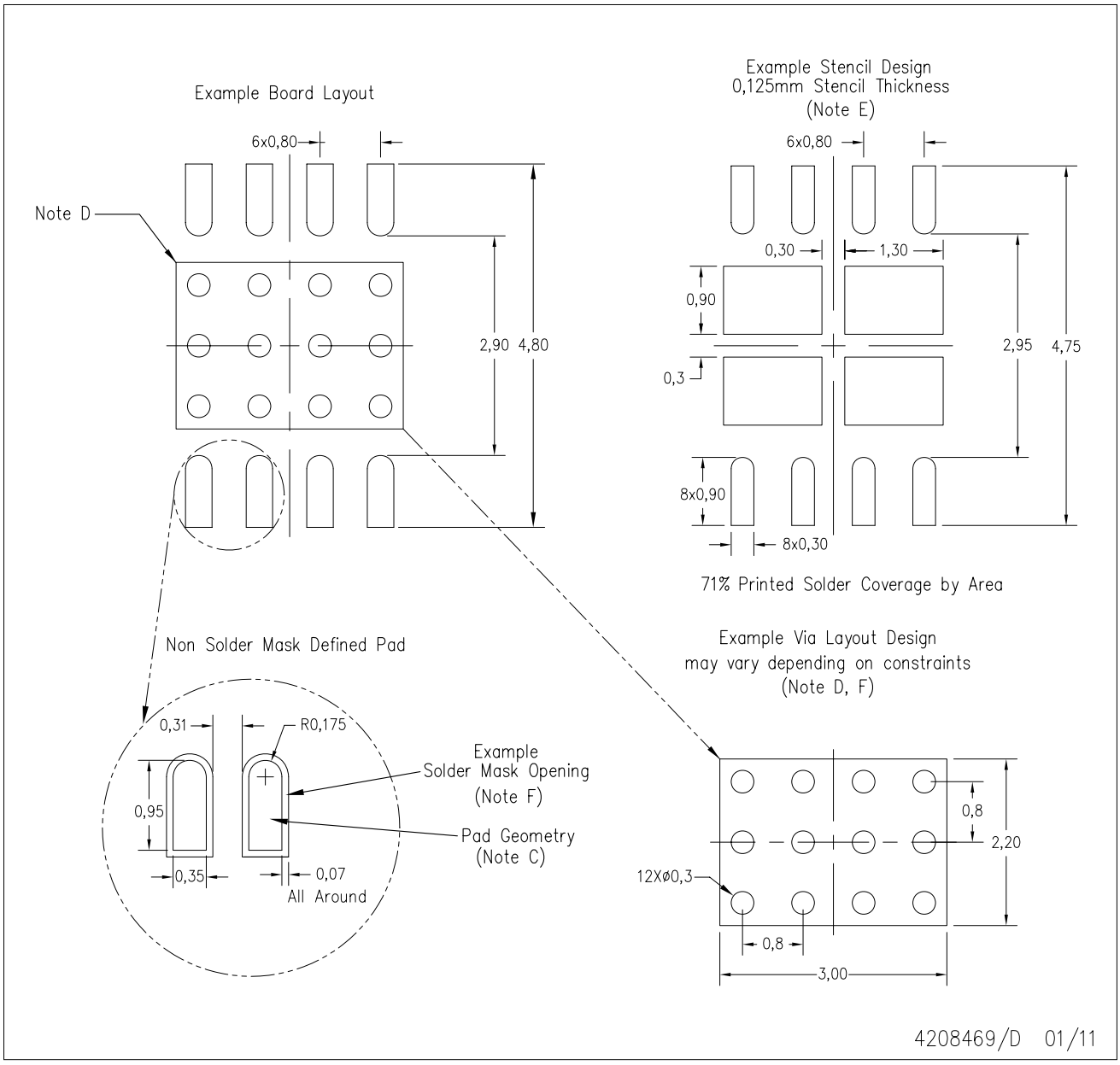
Bottom View

Exposed Thermal Pad Dimensions

4206882/F 01/11

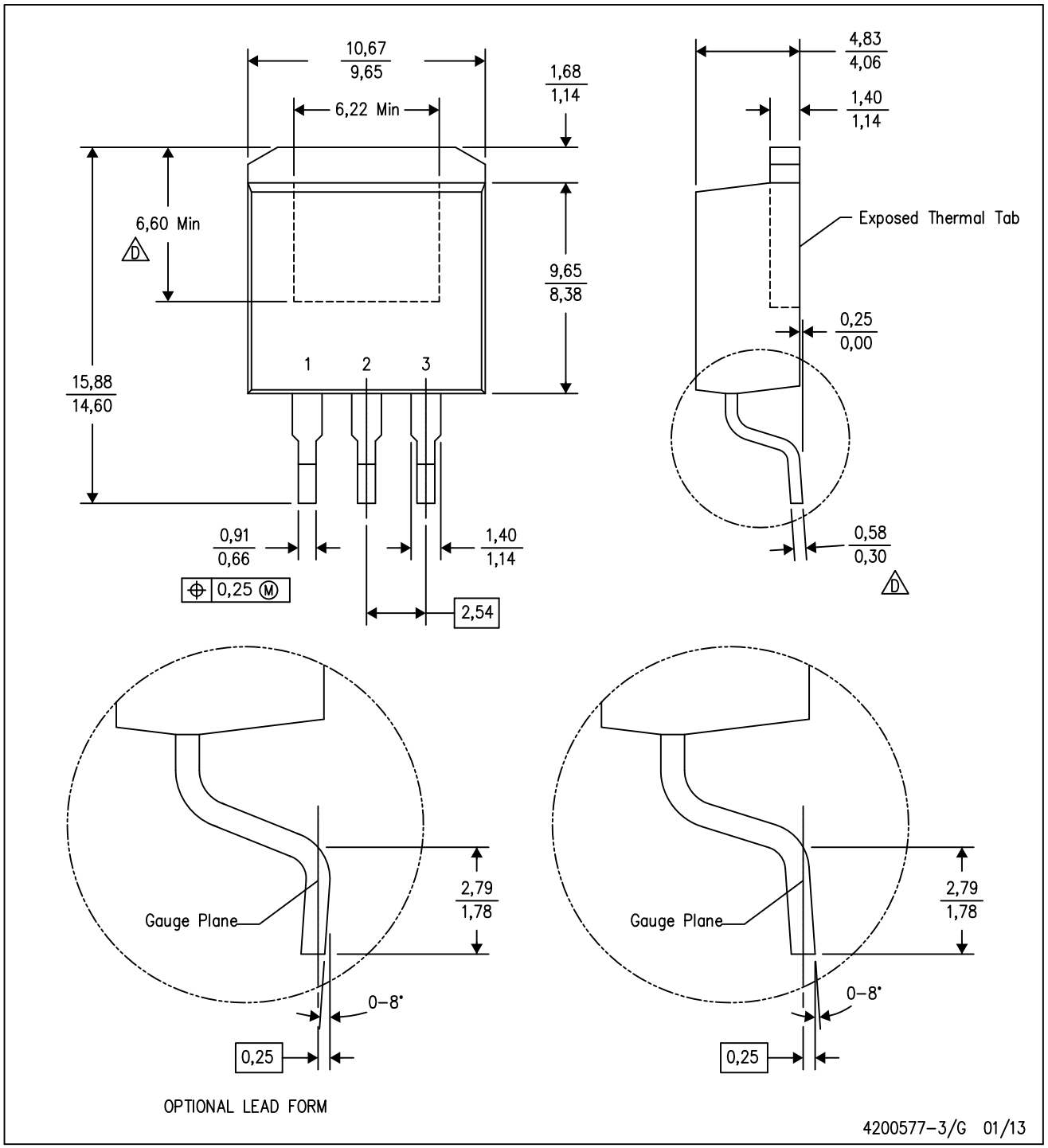
NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



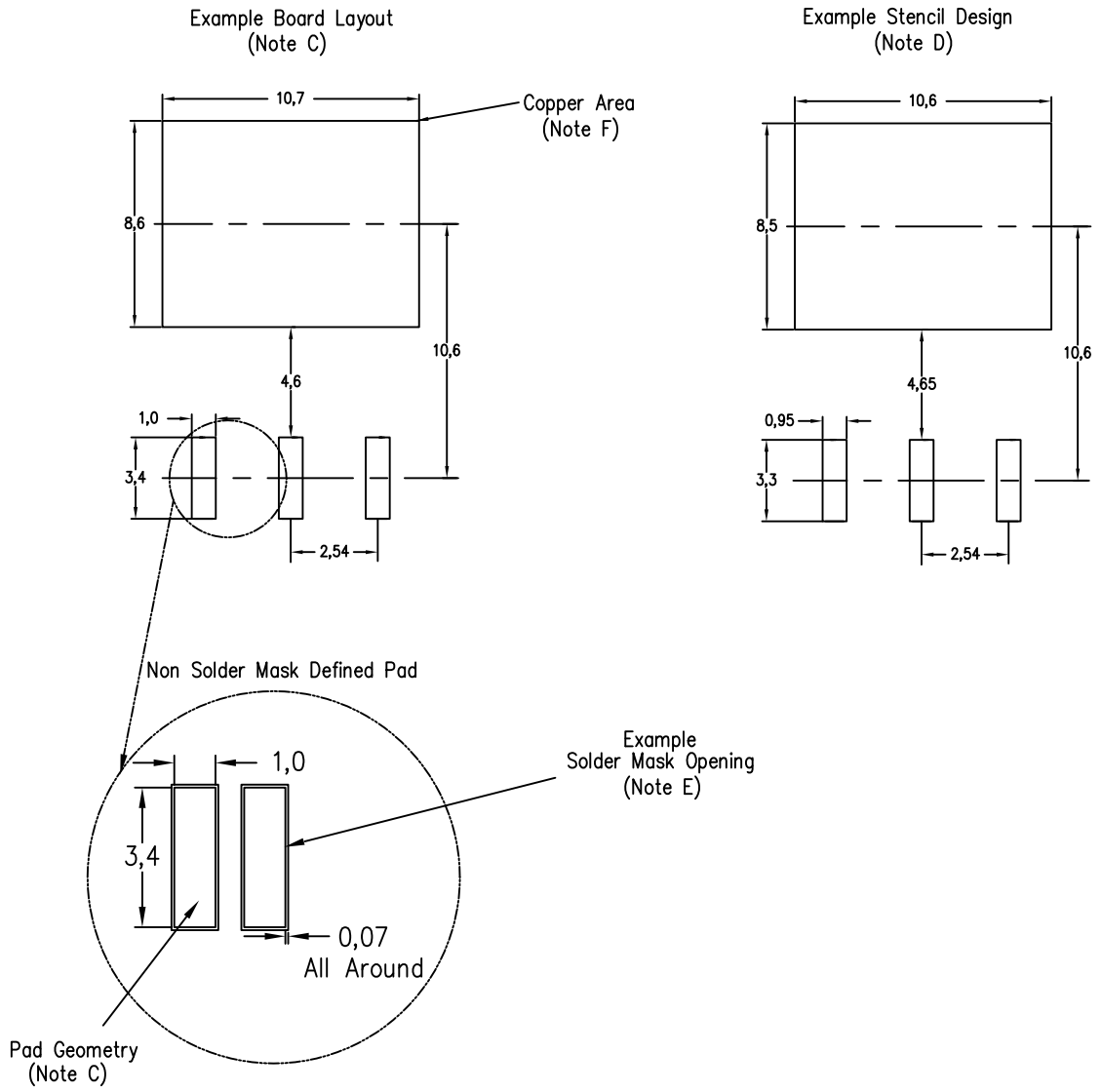
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

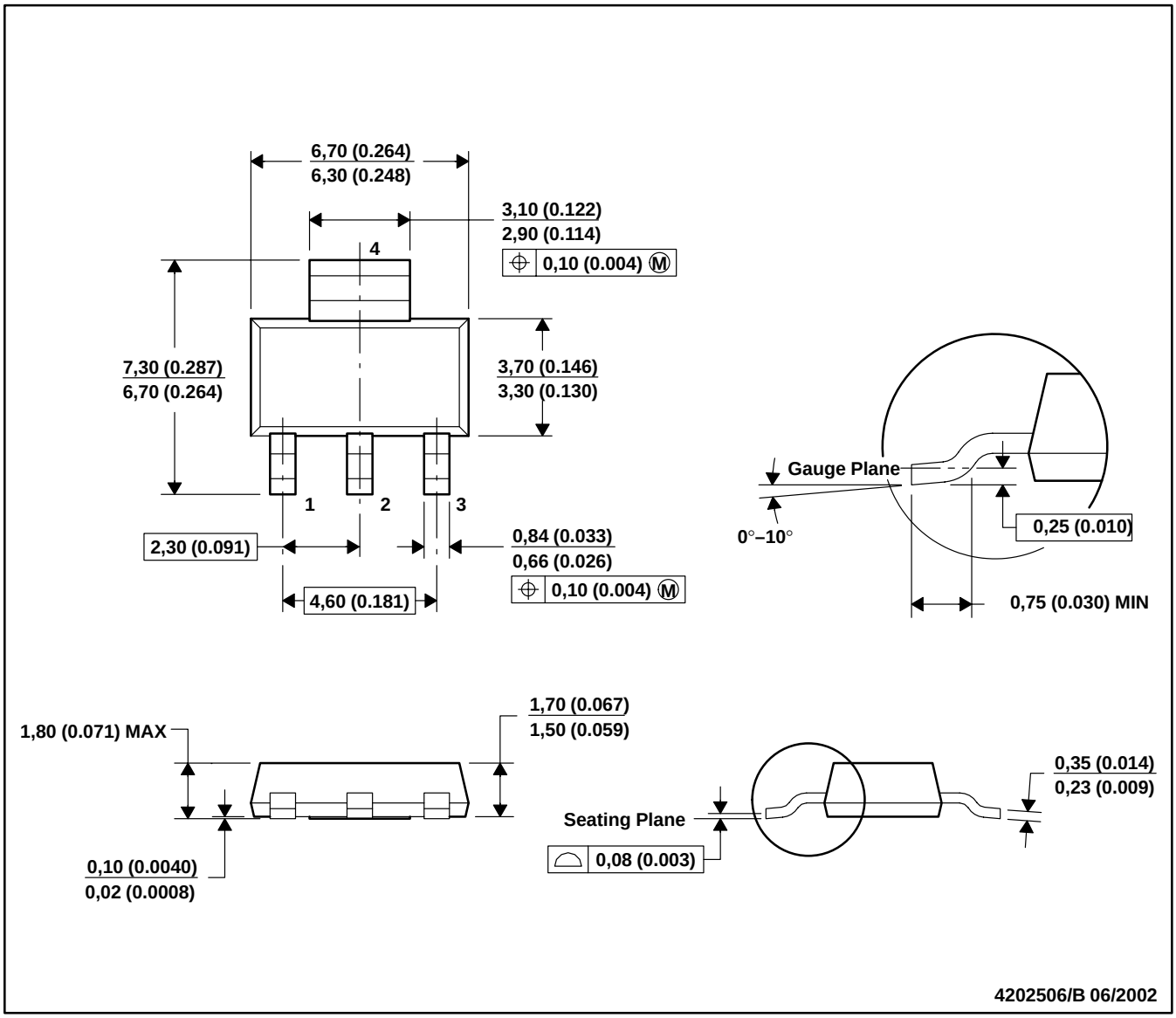
KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

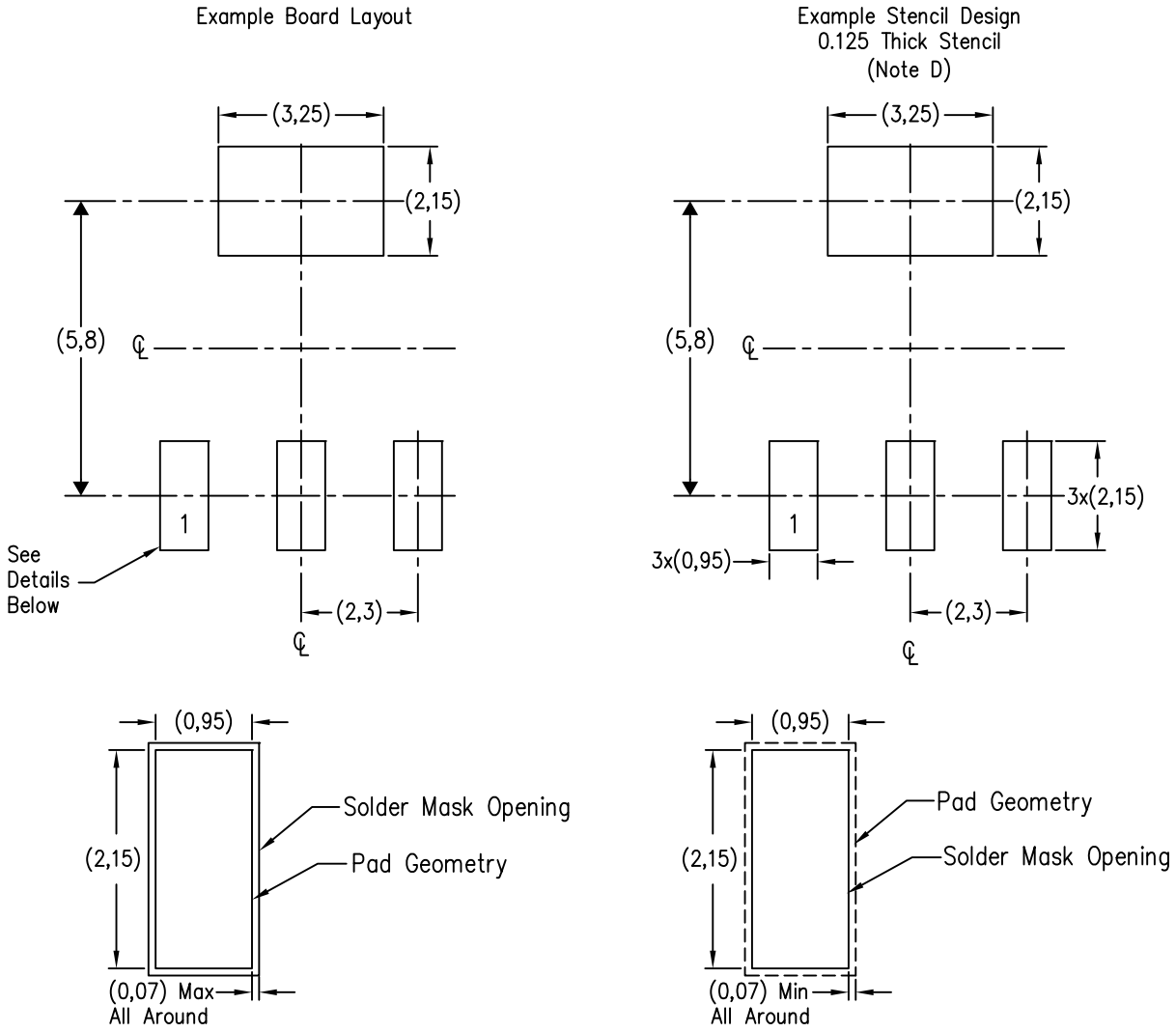
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

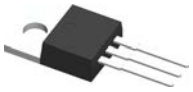
DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

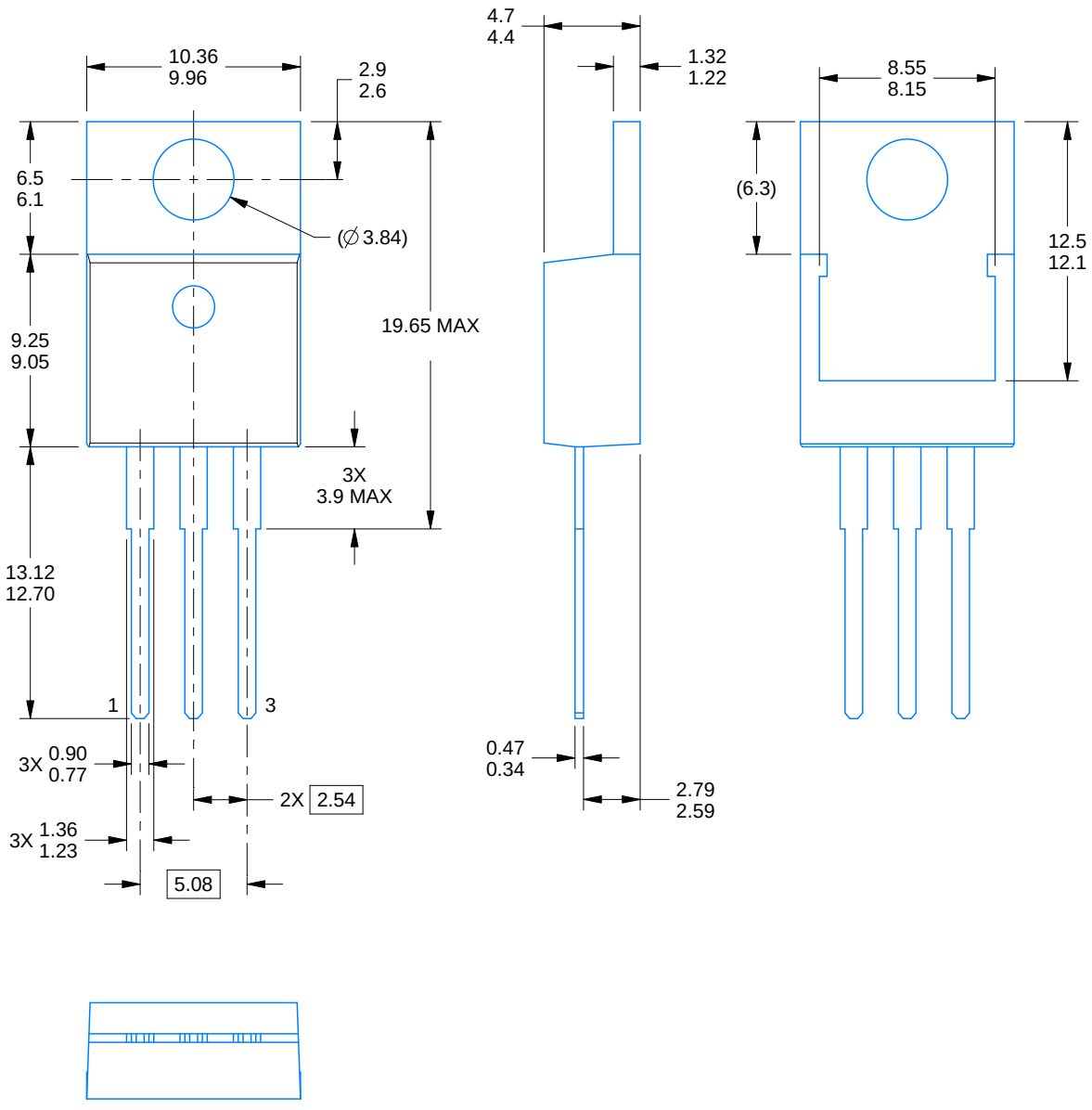
KCS0003B



PACKAGE OUTLINE

TO-220 - 19.65 mm max height

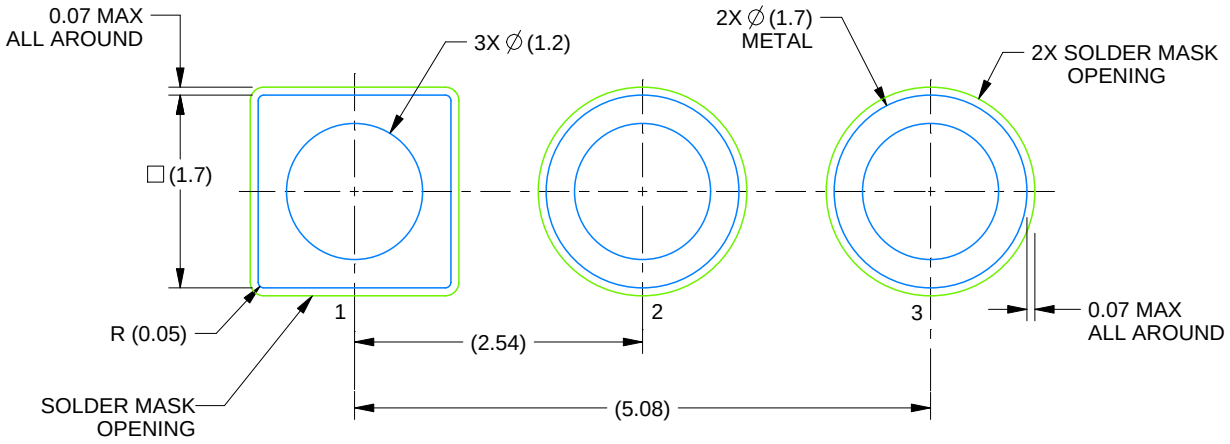
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

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